

Double Patterning for 56 nm Pitch Test Designs Using Inverse Lithography

Thuc Dam, Robert Gleason, Paul Rissman* and Robert Sinn
Luminescent Technologies, Inc., Palo Alto, CA

ABSTRACT

The ITRS roadmap¹ lists double patterning 193 nm immersion exposure with inverse lithography as the likely solution through the 22 nm half pitch generation. Three different patterns, scaled to 56 nm pitch, were explored using inverse lithography.^{2,3} The patterns are a trim mask design adapted from Schenker, et al.⁴, a bit line design published by Pyo, et al.⁵ and a metal layer design published by Lucas, et al.⁶. A free form gray scale illuminator was determined for each pattern. Good results were obtained for the trim mask design with a process variation of less than 8 nm for 50 nm of defocus and MEEF less than 6. The bit line design had to be modified from the published version which increased the pattern area by 18.8%. For this pattern there was a maximum process variation of 11 nm for 50 nm of defocus and MEEF less than 14. The metal layer design had to be modified which increased the pattern area by 2.6%. With these changes there was a maximum process variation of 8.4 nm for 50 nm of defocus and MEEF less than 7.

Keywords: Double patterning, inverse lithography, immersion lithography, source mask optimization

1. INTRODUCTION

The 2009 International Technology Roadmap for Semiconductors (ITRS) roadmap shows a 90 nm MPU metal 1 pitch as achievable using single exposure, 193 nm immersion lithography. To further increase resolution, the ITRS lists double patterning⁴⁻⁹, inverse lithography^{2,3} and source mask optimization (SMO)¹⁰ and these topics have been the subject of active research and a number of publications over the past few years.

In this work the capability of these resolution enhancements is explored on three patterns from the literature. In each case, the patterns have been designed or resized to a pitch of 56 nm, beyond the imaging limit for single layer 193 nm immersion lithography. Each pattern was examined to see if there were any layout conflicts, also known as coloring errors. Redesign to avoid coloring issues usually causes an increase in the overall pattern area, and therefore an increase in cost of manufacturing. In the most extreme case, redesign of the pattern could even negate the advantage of the shrinking the pitch.

When the patterns are split into two layers creating a pitch of 112 nm, the aerial images are sinusoidal. The maximum depth of focus will be achieved when the pattern consists of equal lines and spaces. Once the pattern has been split into two parts, this can be achieved by biasing the data from 28 nm lines and 74 nm spaces to 56 nm equal lines and spaces. After the lithography is complete, an "etchback" step will return the features to the require dimension. The etchback is simulated as a uniform, isotropic resize of the data.

The pattern exposure process was optimized for each design. Improvement in the performance of negative resists has encouraged recent work^{11,12} that show the advantage of bright field masks over dark field masks for many patterns. For each design, bright field vs. dark field, chrome on glass masks and attenuated phase masks were compared. Sub-resolution assist features (SRAFs) can improve the depth of focus and printability of many patterns. However, SRAFs are sensitive to fixed values of mask resize, and can cause the sensitivity of the printed image size to the mask size to increase, as measured by the mask error enhancement factor (MEEF). MEEF is one of the key parameters studied in this work.

* all correspondence to paul@luminescent.com

Inverse lithography is a process that seeks to find the optimal mask to print a given target pattern. While straightforward in concept, the recipe for inverse lithography can strongly influence the quality of results. One part of the recipe generation consists of choosing the emphasis on the different features in the design, such as line ends or smooth areas. These will differ whether the pattern is a cut line design, where the emphasis is on smooth cuts across the line ends, or a contact layer where round features are the expected result. Mask rule constraints (MRC), typically set by requirements of mask manufacturing, can alter the results achieved in subtle ways.¹³ No MRC requirements were set in this study, and all masks used were the native or “curvy” masks produced by the inverse lithography program.

The optimum configuration of the exposure source can be defined in cases when the pattern is a regular array of features, such as a contact array or an array of lines and spaces. In general, as in the case in logic designs, the optimum exposure source cannot be pre-determined from pattern inspection. In this work the source was optimized for each of the patterns using a linear combination of ortho-normal basis functions on the unit disk. The coefficients of the basis functions were optimized based on published direct search methods using the cost function that is normally used for inverse lithography.

2. PATTERNS STUDIED

Schenker et al.⁴ discussed gate patterning technique using lines and spaces that are then trimmed to create the desired pattern, as is shown in on the left of Figure 1. While originally discussed for phase masks, the same approach can be used with a double exposure trim mask method, once the initial layer is defined. The pattern was adapted as is shown on the right of Figure 1.

It was assumed that the first layer, shown in blue in the figure, was defined using a double patterning, phase edge¹⁴, or self-aligned spacers¹⁵ and was not studied. The overlap of the side by side single cuts through the adjacent lines was varied to test the difficulty in imaging the 28 nm by 56 nm features.

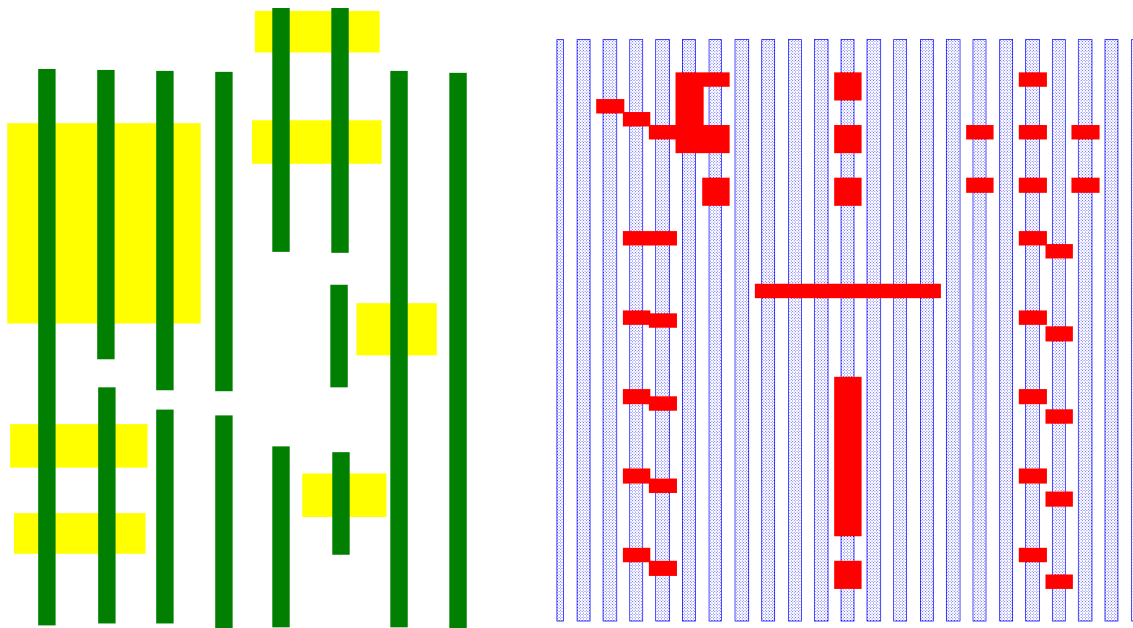


Figure 1 - Cut line pattern (right) adapted from Schenker, et al.⁴, (left).

Pyo, et al.⁵ described a bit line design (Figure 2), which is colored into two layers. The red circles indicate potential problem regions for the design.

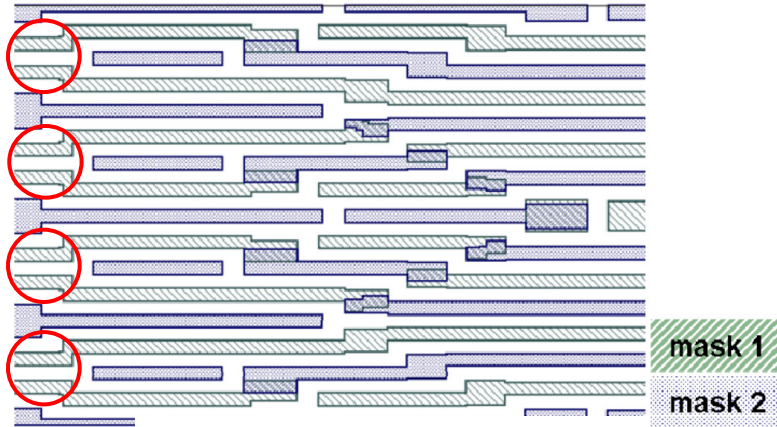


Figure 2 - Bit line design from Pyo, et al.⁵

Lucas, et al.⁶ described a metal layer design shown in Figure 3. In their paper, the authors observe issues with line ends and overlaps as is shown in the figure. There is a coloring problem shown in the green circled area and a complicated overlap circled in brown. These issues will be addressed in the results below.

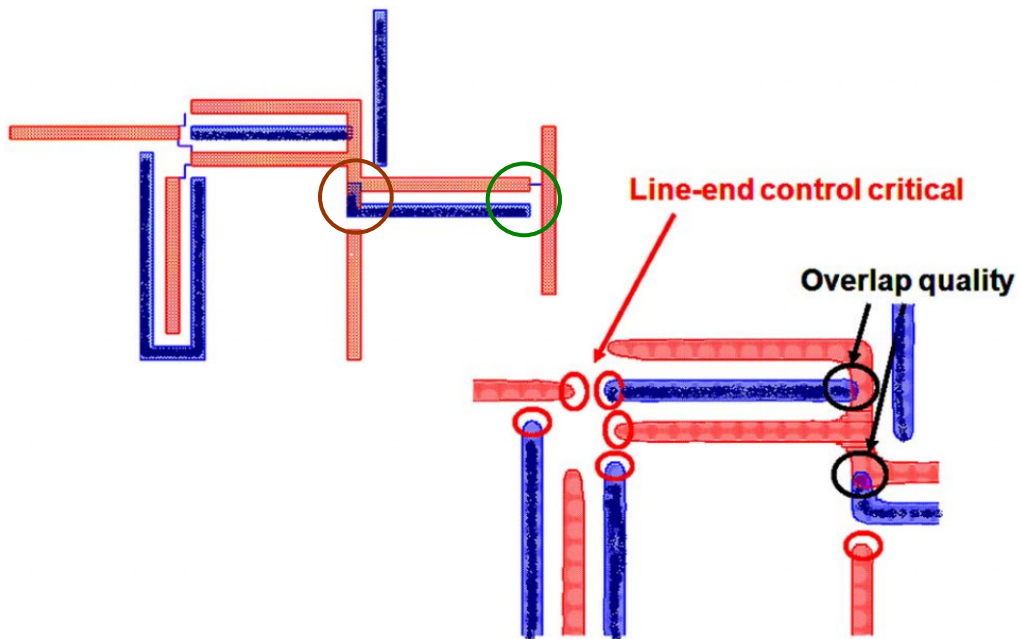


Figure 3 - Metal line design from Lucas⁶.

3. RESULTS

3.1 Cutline Pattern

The cutline design mask and gray scale, custom source are shown in Figure 4. The dark lines in mask indicate the original design contours and the green areas indicate the opaque regions of the mask. The best results were achieved using a bright field, attenuated mask, meaning negative resist would be required to achieve the required resist pattern. With a dark field mask features were missing in the printed image. The source image shows the areas of maximum

intensity (red) and zero intensity (dark blue). The lighter colors (yellow, green, light blue), indicate intermediate source intensity. The source uses x-y polarization to enhance the corners of the printed image.

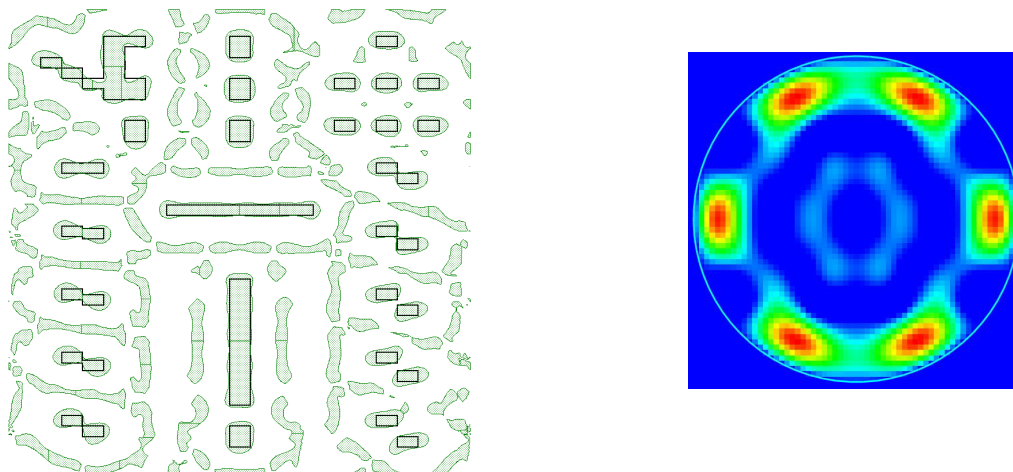


Figure 4 - mask and source for cutline design.

Figure 5 shows the printed image from the mask and source shown in Figure 4. The black contours are the targets, red shows the best focus image and green shows the image for 50 nm of defocus. Contours of horizontal features that cover two or more of the lines being cut are smooth, and meet the design goal. Single 28 by 56 nm features tend to be more curved, which could lead to high field regions in the resulting gate line ends. Table 1 lists the data from a number of cutlines, typically the worst case regions. The maximum edge placement error (epe) is 6 nm at cutline 9. The maximum process variation (pv) for 50 nm of defocus is 8.6 nm at cutline 2, which is strongly influenced by the adjacent features. The maximum meef1 (for -0.1 nm of mask resize) is 6.0 at cutline 2 and the maximum meef2 (for +0.1 nm of mask resize) is 4.3 at cutline 9. The image log slope (ils) is 0.02-0.04 nm⁻¹ for this pattern.

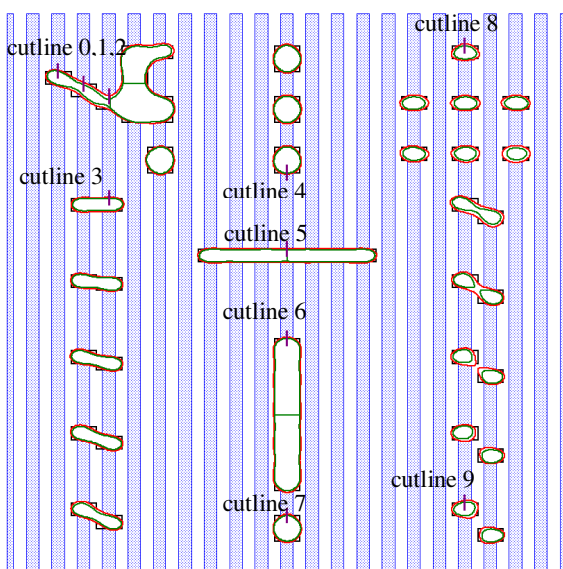


Figure 5 - Image from mask and source in Figure 4.

cut-line	epe (nm)	ils (nm ⁻¹)	pv(nm) - 50 nm df	meef1	meef2
0	2.82	0.030	2.45	1.67	3.33
1	3.32	0.022	5.05	2.74	2.84
2	3.11	0.016	8.58	5.93	6
3	2.14	0.036	2.28	2.33	2.52
4	-2.85	-0.038	2.28	1.67	1.74
5	0.83	0.038	2.12	2.26	2.34
6	2.35	0.034	2.45	1.97	2.05
7	3.69	0.028	3.41	2.52	2.66
8	4.59	0.026	4.29	3.00	3.12
9	6.05	0.025	3.92	4.13	4.31

Table 1 - Lithography data for the cutline mask.

3.2 Bit Line Pattern

The bit line design in Figure 2 is improperly colored in the regions circled in red, since there are 56 nm pitch features on the same mask layer, and as shown in on the left of Figure 6, the areas did not image properly. The pattern was redesigned to eliminate the areas of poor imaging on the first mask layer (red) as shown on the right in Figure 6. In addition, line end spacing on mask 2 (blue) was increased to 56 nm to improve line end performance and MEEF at the areas circled in green. Finally, the mask 1 and mask 2 overlap in the region circled in brown was removed since there was a coloring issue on mask 1. In addition, the line on mask 2 in this area was extended to ensure continuity. These changes increased the overall size of the pattern by 18.8% over the original design.

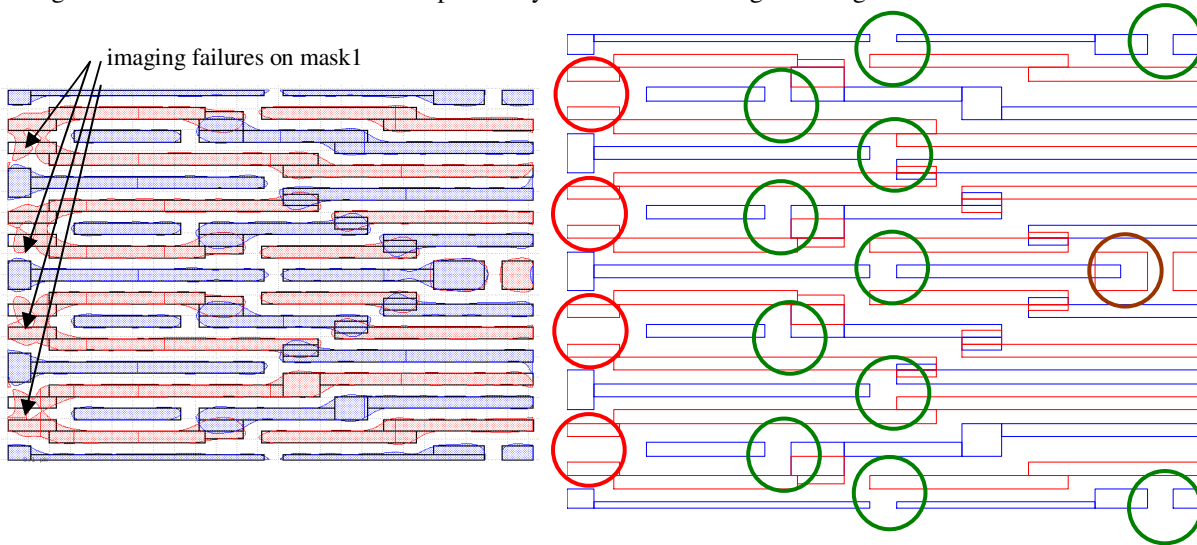


Figure 6 - Imaging failures in the original design (left) and the pattern redesign (right).

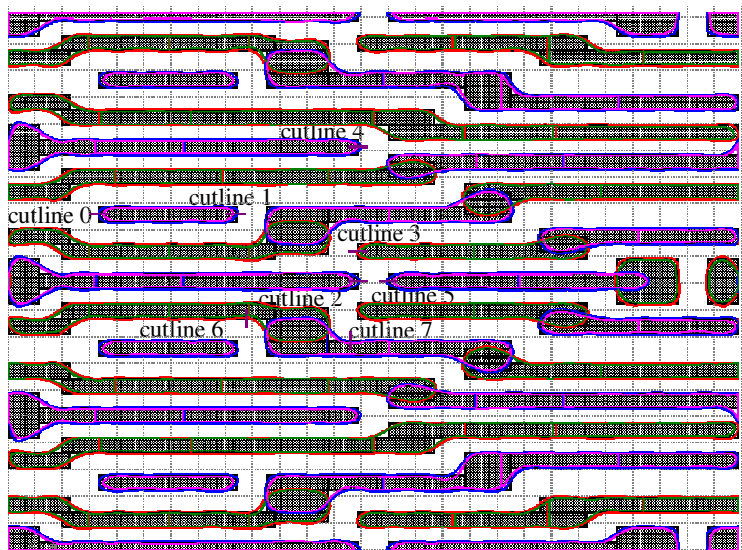


Figure 7 - Image of the revised bit line pattern.

cut-line	epe (nm)	ils (nm ⁻¹)	pv(nm) - 50nm df	meef1	meef2
0	-1.19	-0.012	9.98	7.99	8.67
1	0.98	0.011	8.44	7.93	8.31
2	2.19	0.007	11.09	13.6	14.0
3	-1.31	-0.012	7.45	7.37	8.30
4	1.57	0.012	6.08	7.35	8.39
5	-0.76	-0.010	10.4	9.76	10.3
6	0.92	-0.022	4.51	4.35	3.72
7	-2.49	0.021	5.12	4.30	4.31

Table 2 - Lithography data for revised bit line pattern.

Figure 7 shows the imaging results for the revised bit line pattern. The red and blue contours are best focus results and green and pink contours are for 50 nm of defocus. The maximum epe is 2.2 nm for cutline 2. The worst pv is 11 nm for

50 nm of defocus was at cutline 2, dominated by line end pullback. This cutline is also the most sensitive for MEEF, with 14. IIs for this pattern is 0.007 to 0.022 nm⁻¹.

3.3 Metal Layer Pattern

The area circled in red in Figure 3 is colored incorrectly due to the minimum spacing between the horizontal and vertical lines on layer 1 (red). Correcting this problem by increasing the spacing between the features increased the overall chip area by 5.1%. A second approach is to split the vertical line. This approach gives good results for best focus as shown in Figure 8.

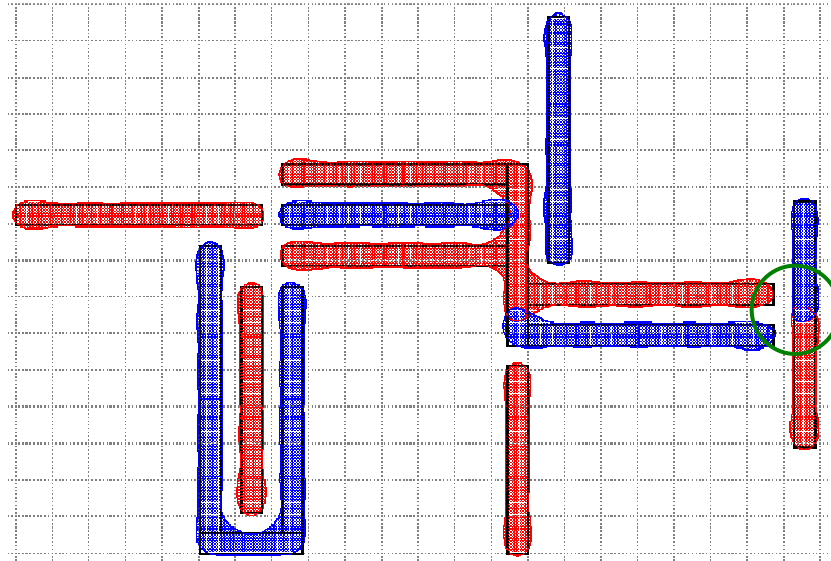


Figure 8 - Metal layer pattern split to correct the coloring issue shown in Figure 3.

The pattern modification resolved the coloring issue. A second issue with this pattern is how to optimize the pattern overlap and is illustrated in Figure 9. The leftmost curves show the overlap as originally designed. Other approaches are to change the overlap from only an extension of the red layer to only an extension of the blue layer. The most successful approach is the right hand image which maximizes the contact area between the layers while minimizing the area of bridging between the lines. The minor “peanutting” on the left of the extension region is not an issue.

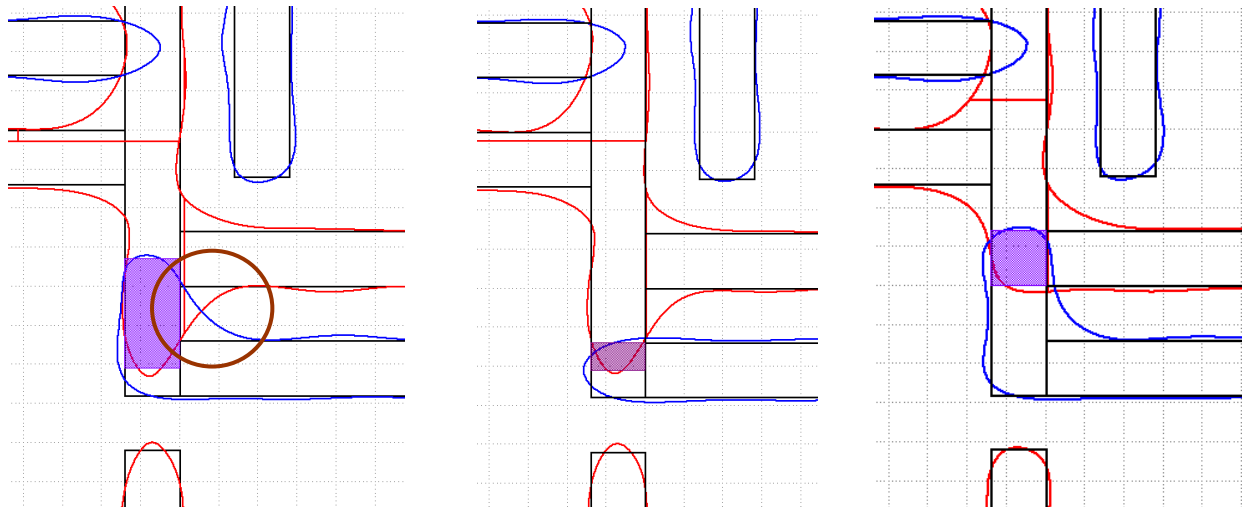


Figure 9 - Optimization of the overlap circled in Figure 3.

To improve the process margin for this pattern, the individual layers were sized up by 14 nm, to create 56 nm equal lines and spaces, as is shown in Figure 10a. However, while improving the depth of focus, bridging after the “etch” of the patterns circled in red, necessitated resizing the spaces where the pattern bridged in Figure 10b. This increased the overall pattern area by 2.6%.

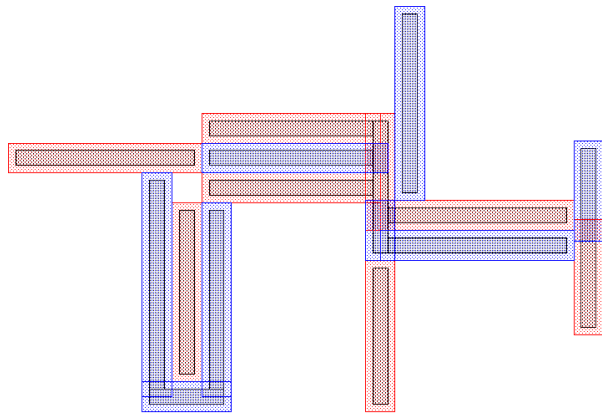


Figure 10a - Metal pattern oversized by 14 nm to create equal lines and spaces.

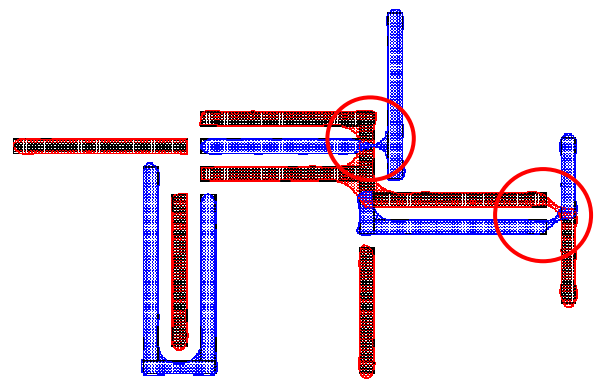


Figure 10b - Areas of bridging after the pattern “etch”.

The best results for the metal layer pattern were obtained using bright field, attenuated masks. The modified pattern images are shown in Figure 11. The black contour is the target and red and blue contours are best focus results for layer 1 and layer 2. The green and pink contours are the images for 50 nm of defocus. The worst epe is 6.0 nm at cutline 3, although there is sufficient overlap that this is not an imaging issue. The worst process variation with 50 nm of defocus is 8.4 nm at cutline 4. MEEF is less than 7 for this pattern.

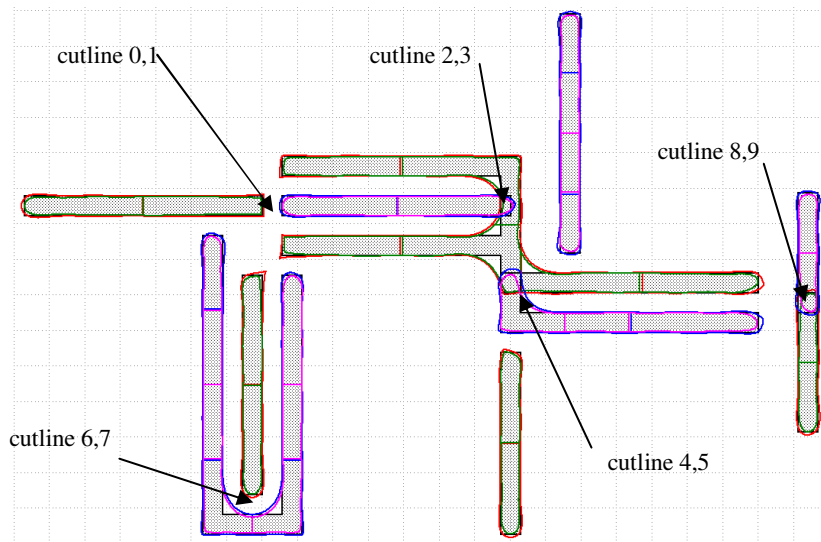


Figure 11 - Metal layer pattern after redesign to eliminate bridging.

cut-line	epe (nm)	pv(nm) - 50nm df	meef1	meef2
0	1.66	2.74	6.90	7.10
1	3.65	4.40	3.65	4.40
2	0.41	4.21	3.00	3.20
3	6.07	3.24	5.60	5.85
4	5.59	8.41	5.60	5.85
5	1.71	2.59	4.48	4.80
6	2.46	4.91	2.86	3.10
7	3.05	5.18	3.15	4.50
8	4.24	4.73	1.50	1.70
9	0	3.97	3.07	2.32

Table 3 - Lithography data for the revised metal line pattern.

4. CONCLUSIONS

Three complex designs from the literature, a cutline pattern, a bit line pattern and a metal layer pattern, were studied at 56 nm pitch using double layer patterning, optimized gray scale illumination and inverse lithography. Good results were obtained for each of the patterns, although the bit line and metal patterns had to be modified to eliminate coloring issues and line end problems. Depth of focus for the metal layer pattern was improved by oversizing the data before mask optimization and using a simulated etch to resize the layers after image definition.

REFERENCES

- [1] <http://www.itrs.net/links/2009ITRS/Home2009.htm>
- [2] Saleh, B.E.A. and Sayegh, S.I., "Reduction of errors of microphotographic reproductions by optimal corrections of original masks", *Optical Engineering* 20, 781-784 (1981).
- [3] Abrams, D. and Pang, L., "Fast Inverse Lithography Technology", *Proc. of SPIE* 6154, 61541J, 61541J-1-9 (2006).
- [4] Schenker, R., Singh, V., and Borodovsky, Y., "The role of strong phase shift masks in Intel's DFM infrastructure development", *Proc. of SPIE* 7641, 76410S-1-9 (2010).
- [5] Pyo, Y.-J., Choi, S.-H., Park, C.-H., Lee, S.-H., Yoo, M.-H., and Kim, G.-T., "Statistical approach to specify DPT process in terms of patterning and electrical performance of sub-30nm DRAM device", *Proc. of SPIE* 797413, 797413-1-7 (2011).
- [6] Lucas, K., Cork, C., Miloslavsky, A., Luk-Pat, G., Barnes, L., Hapli, J., Lewellen, J., Rollins, G., Wiaux, V., and Verhaegen, S., "Double-patterning interactions with wafer processing, optical proximity correction, and physical design flows", *J. Micro/Nanolith. MEMS MOEMS*, 8, 033002-1-10 (2009).
- [7] Jessen, S.W., Prins, S.L., Blatchford, J.W., Dillon, B.W., and Proglor, C.J., "Exploring Complex 2D Layouts for 22 nm Node Using Double Patterning/Double Etch Approach for Trench Levels", *Proc. of SPIE* 7641, 76410A-1-12 (2010).
- [8] Zeggaoui, N., Farys, V., Trouiller, Y., Yesilada, E., Robert, F., and Besacier, M., "Optimization of double patterning split by analyzing diffractive orders in the pupil plane", *Proc. of SPIE* 7823, 78233Y-1-8 (2010).
- [9] Liebmann, L., Pietromonaco, D., and Graf, M., "Decomposition-Aware Standard Cell Design Flows to Enable Double-Patterning Technology", *Proc. of SPIE* 7974, 79740K-1-12 (2011).
- [10] Rosenbluth, A.E., Bukofsky, S., Hibbs, M., Lai, K., Molless, A., Singh, R.N., and Wong, A., "Optimum Mask and Source Patterns to Print a Given Shape", *Proc. SPIE* 4346, 487-502 (2001).
- [11] Brunner, T.A. and Fonseca, C., "Optimum tone for various feature types: positive versus negative", *Proc. SPIE* 4345, 30-36 (2001).
- [12] Sinn, R., Dam, T. and Gleason, B., "Comparison of Clear-Field and Dark-Field Images with Optimized Masks", *Proc. SPIE* 7973, 79731V-1-8 (2011).
- [13] Dam, T., Sinn, R., Rissman, P. and Gleason, B., "Exploring the impact of mask making constraints on double patterning design rules", to be presented at Photomask Technology September, 2011.
- [14] Liu, H.-Y., Su, C.-Y., Farrar, N., and Gleason, B., "Fabrication of 0.1 μm T-shaped gates by phase-shifting optical lithography", *Proc. SPIE* 1927, 42-52 (1993).
- [15] Choi, Y.-K., King, T.-J., and Hu, C., "A Spacer Patterning Technology for Nanoscale CMOS", *IEEE Trans. on Elect. Dev.* 49, 436-441.