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Enhancing Fullchip ILT Mask Synthesis Capability for IC Manufacturability

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ABSTRACT

It is well known in the industry that the technology nodes from 30nm and below will require model based SRAF / OPC for critical layers to meet production required process windows. Since the seminal paper by Saleh and Sayegh[1][2] thirty years ago, the idea of using inverse methods to solve mask layout problems has been receiving increasing attention as design sizes have been steadily shrinking. ILT in its present form represents an attempt to construct the inverse solution to a constrained problem where the constraints are all possible phenomena which can be simulated, including: DOF, sidelobes, MRC, MEEF, EL, shot-count, and other effects. Given current manufacturing constraints and process window requirements, inverse solutions must use all possible degrees of freedom to synthesize a mask.

Various forms of inverse solutions differ greatly with respect to lithographic performance and mask complexity. Factors responsible for their differences include composition of the cost function that is minimized, constraints applied during optimization to ensure MRC compliance and limit complexity, and the data structure used to represent mask patterns. In this paper we describe the level set method to represent mask patterns, which allows the necessary degrees of freedom for required lithographic performance, and show how to derive Manhattan mask patterns from it, which can be manufactured with controllable complexity and limited shot-counts. We will demonstrate how full chip ILT masks can control e-beam write-time to the level comparable to traditional OPC masks, providing a solution with maximized lithographic performance and manageable cost of ownership that is vital to sub-30nm node IC manufacturing.

Keywords: ILT, OPC, manufacturable, SRAF

1. INTRODUCTION

In this paper we will discuss some aspects of how Luminescent has constructed and solved the mask correction problem using inverse problem methods. The study of Inverse Lithographic Technology (ILT) by numerous research groups at universities and companies has lead to many interesting results. However, there have been very few which show the applicability of these methods to real full chip production sized use.

Luminescent's version of ILT is formulated using the level set method for tracking interface movement (mask edges). The optimization problem of correcting the mask is formulated as an inverse problem which can be solved using some functional analysis and numerical solvers. Many details about the level set method and ILT have been previously published [3], so we will not repeat them in detail here. We will however attempt to explain some of the most critical algorithms and techniques which allow ILT to be extended to full chip mask synthesis. First we will describe the model, as it is the foundation upon which computational lithography is built. Then we describe the mask synthesis procedure from the higher level distribution of work, to the lower level lithographic and geometric controls we use.

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2. MODELING

In this section we review the modeling approach used in full chip ILT mask synthesis.

2.1 Model Formulation

The frequency domain formulation of the lithography model capturing mask, optical, and resist effects is [4]

$$I = \left(G \bullet \int M^{*} \bullet B^{*} \bullet TCC \bullet B \bullet M\right) + L \bullet M$$

Where ***I*** is image intensity inside resist, ***G*** represents resist effects, ***M*** is mask spectrum, ***B*** represents mask effects, ***TCC*** is Hopkins transmission cross coefficients, ***L*** represents micro-loading effects. Here the $\bullet$ is convolution (frequency product) and the $\int$ is an integral over the frequency domain. The model formulation is amenable to the level set based inverse problem formulation we use, as we can compute the analytic functional derivative of the cost function when the model is of this form.

2.2 Model Calibration

The model calibration [5] is a combination of global search and local search of the minimum cost function, which is the Sum-of-Squared-Errors between simulated CDs and measured CDs over a list of test patterns. The local search is further constrained by using an active-set method.

3. MASK SYNTHESIS

In this section we will give an overview of the complete ILT mask synthesis flow. The input to the flow is a lithography model, a target design, and some ILT specific recipe parameters which govern the lithographic and geometric controls and constraints. The output will be a mask which has been optimized to meet these controls.

3.1 Outline of Flow

Here we will give an outline of the full chip mask synthesis flow.

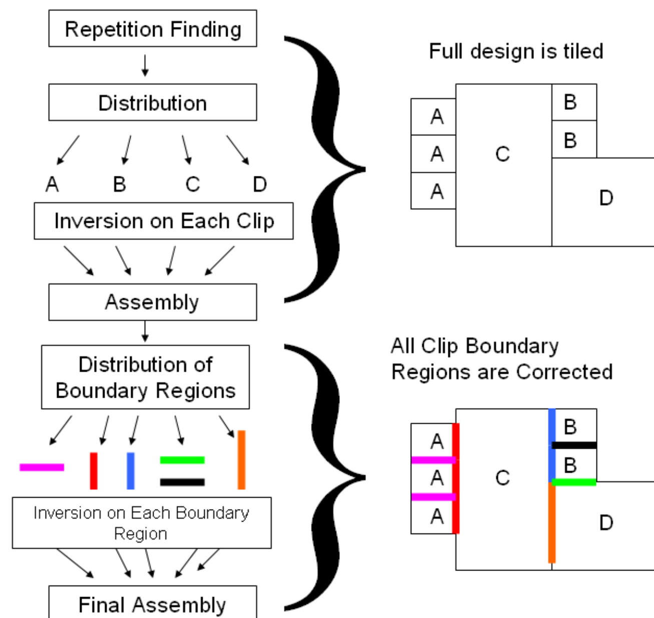

Figure 1. ILT flow.

3.2 Parallelization

The ILT flow is a multi-pass distributed processing algorithm. The initial step is repetition finding. The entire result is tiled with unique templates or work units, each of which includes a halo of neighboring shapes. The maximum and minimum work unit sizes are controlled. Maximums are enforced because when the work units are distributed we will have memory restrictions. The actual maximum work unit size in square nm will be primarily dependent on the desired pixel size, as the pixel arrays used in the modeling dominate the memory usage. Minimums are enforced so that the overhead of the halo will not dominate the computational time. This repetition finding method can be run in a parallelized way also.

Once the work units are constructed they are parallel processed on a multi-node machine. On each work unit a sequence of raw mask and Manhattan mask inversions are done, which will be described further in sections 3.3, 3.4. When these are finished they are reassembled into the full design. There will be some work unit boundary mismatch introduced by numerous noise factors such as pixel placement, non-uniqueness of solutions, and interactions which are larger than the halo size. These must be repaired in a localized way near the original work unit boundaries.

The boundary regions are then distributed (each with a local halo) and repaired. These generally have much smaller size than the original work units and run in orders of magnitude less time. There is a blending which is done from the center of these work units (the boundaries of the original set of work units) to their edges; the center has the most correction while the edges are frozen. This guarantees that when these final work units are placed into the final design they will not ruin the results from the originally processed clips.

3.3 Lithographic Controls

The lithographic controls define the cost function, C(mask), which drives the mask evolution.

$$C(mask) = \sum_{d,f,b} w_{dfb} \left(\sum_{p} w_p D(I_{dfb}(p), T(p)) \right)$$

Equation 1. Lithographic cost function. The indices d,f,b are dose, focus, mask bias conditions of image I_{dfb}. w_{dfb} is the weight used for image I_{dfb} , and w_p is the weight applied at pixel p. The design target is T, and D is a metric function to measure the error at pixel p between I and T.

Equation 1 describes the lithographic cost function used to control the mask evolution. The form of the metric D can vary and include almost any type of function. Using level set methods one can derive a gradient of C with respect to the mask if D has certain differentiable properties, and take advantage of using gradient based optimization methods. However, even if D is non-differentiable we can use non-gradient based methods, which have their own merits [6].

The prescription of the location based weights, w_p, can take many factors into account such as local geometry, or other characteristics of the design. It is through these weights that the user can emphasize or deemphasize certain regions of the design. The way we control the location weights is through an interface that is similar to a DRC select operation. Design polygon edges may be selected based on local width, spacing, edge length, neighboring geometry, and other criteria. They can also be selected by an input gds layer. Through these controls the user is able to fine tune the cost function to control the inversion effort given to various regions. Figure 2 shows how some of these selection criteria can be combined to specifically select certain edges of a design.

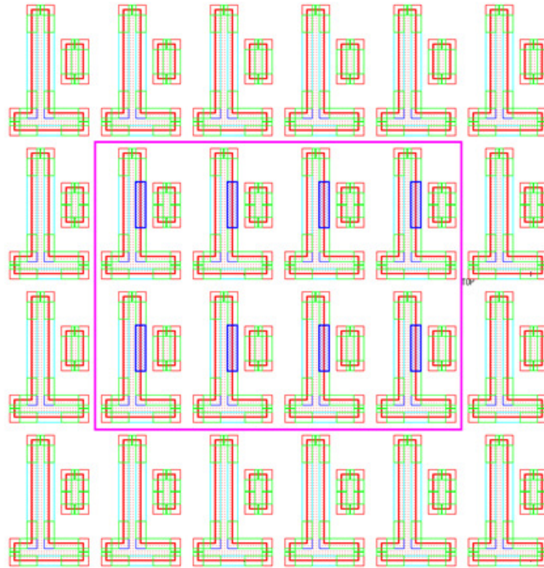

Figure 2. Localized weight markers based on edge length, input gds box layer, and neighboring edge lengths.

3.4 Geometric Controls

The set of first geometric constraints which must be met are the mask rules (MRC). For the raw mask inversion procedure we must approximate the true MRC rules on a smooth mask that has no distinct “edges” and “corners”. For this we rely on various image processing techniques which can extract skeletons of contours, and use these to approximate the widths and spaces of various mask features [7].

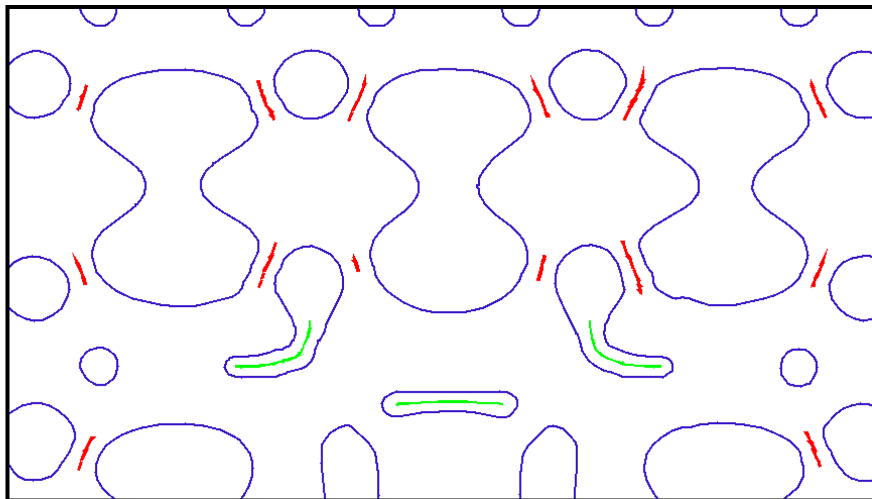

Figure 3. Skeletons used in MRC processing of raw mask. Blue: raw mask edge, green: interior skeleton (width), red: exterior skeleton (spacing).

Besides the standard MRC rules which must be met, there are numerous other controls which are available to the user. The portion of the mask cost under the user’s control is the shot count, and there are numerous tunable controls which make a range of solutions possible [8][9]. In contrast with standard OPC engines which segment the target design before correcting the mask, ILT allows the segmentation to be done automatically using the raw mask as a guide for segmentation placement and size. This can be further enhanced by using lithographic performance to guide the segmentation by using metrics such as the local MEEF as a guide for segmentation coarseness.

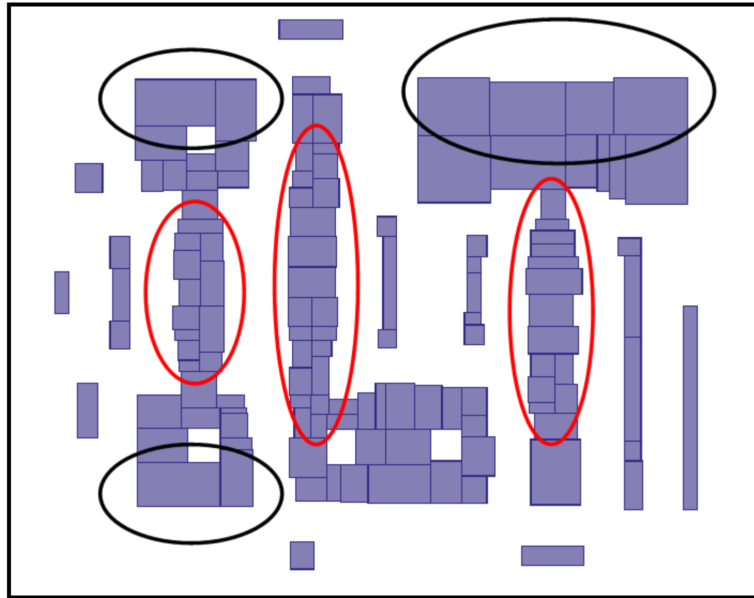

Figure 4. Automated variable segmentation. Red ovals: finer segmentation on narrow lines, black ovals: coarser segmentation on larger pads.

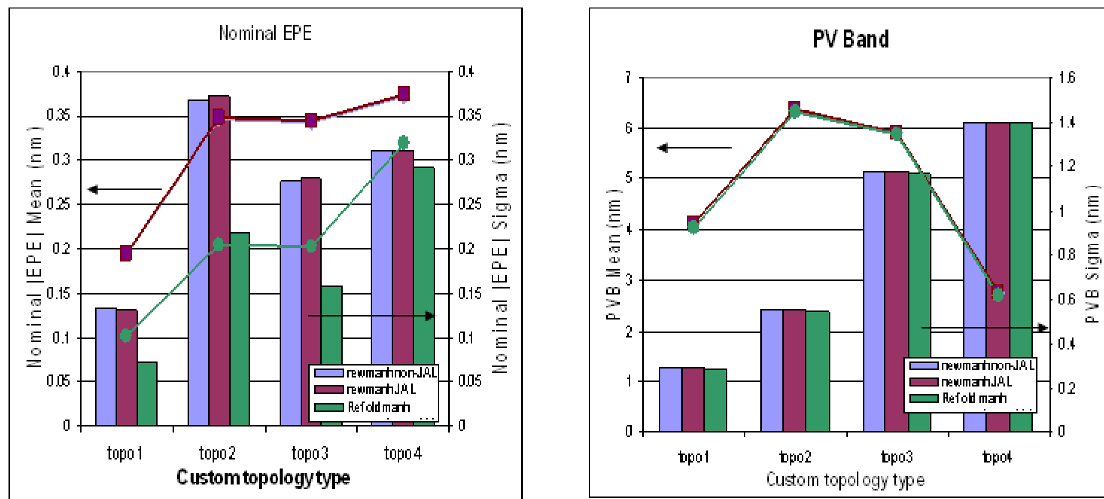

Figure 5. Lithographic effect of Manhattan simplification on 4 sample designs (topology types). Green: baseline, Blue: simpler segmentation, Red: simpler segmentation plus jog alignment. Left: nominal EPE. Right: PV band between nominal and defocus image.

We note that after conversion from the raw mask to the Manhattan mask we still do further mask correction on the edges, adjusting for any errors introduced in the initial conversion from raw to Manhattan mask.

As can be seen in figure 5 there is clearly a first order effect of degraded nominal EPE performance when using simpler masks, but the process window is unaffected. The mask simplification does not fundamentally change the lower frequency effects determined by main feature and sraf size and placement, as it only perturbs the boundaries of these mask shapes. Thorough studies have been done in collaboration with fracturing companies and mask shops which show that ILT mask write times can approach traditional OPC times and are well within required level needed for production [8][9].

3.5 Optimization Methods

The optimization methods used are those designed for constrained nonlinear problems. Customizations have been made to off the shelf algorithms to enhance the speed and allow for a more robust solution that can more frequently approach the global minimum.

One critical area which largely determines the optimization speed is the quality of the starting mask which is fed into the optimization algorithm[10][11]. Currently we have two alternate methods for generating a starting mask. The first is based on an evaluation of the cost function and its gradient. This method is somewhat related to other published model based SRAF methods which rely on various types pixel information produced by the simulation engine. The second method is to use a hybrid approach where lithographic information is precalculated and encoded as a set of parameters, which are then used in conjunction with the design layout to generate an initial mask. This method is more easily tuned to control mask complexity, and numerous experiments can be run to compute an optimal parameter set. In either case the robustness of the optimization algorithm which follows the initial mask construction is what largely determines the quality of the final mask.

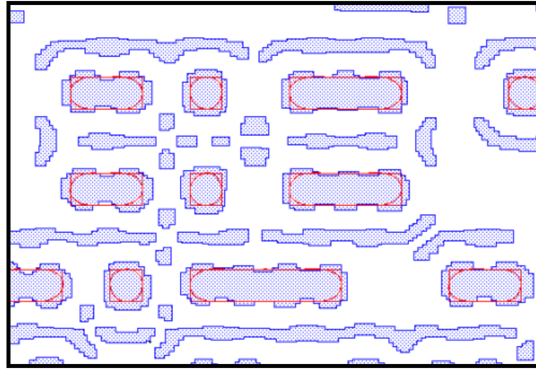

Figure 6. Examples of ILT handling of geometric and lithographic conflicts when sraf placement is complicated. There are many competing requirements such as MRC, MEEF, and sidelobe control which must be taken into account.

3.6 Localized OPC Repair/Replacement

A more recent option that has been implemented is to either repair or replace an OPC mask in a localized region (which may be arbitrarily large) with ILT [12], see also [13]. This has been tested on some customer cases. The idea here is to use either design space checks or ORC to identify areas where OPC has difficulty and to apply ILT specifically to those regions. While it is necessary to match ILT and OPC models, in practice this has not been a difficult issue. Also, the blending of the ILT and OPC masks at the design split boundaries is handled by ILT and described in more detail in the ILT Hotspot (HSF) paper.

The main benefits of this method are to allow the user to gain the lithographic advantages that ILT produces on the most difficult regions, while using the more familiar and expedient OPC method on the remainder of the layout.

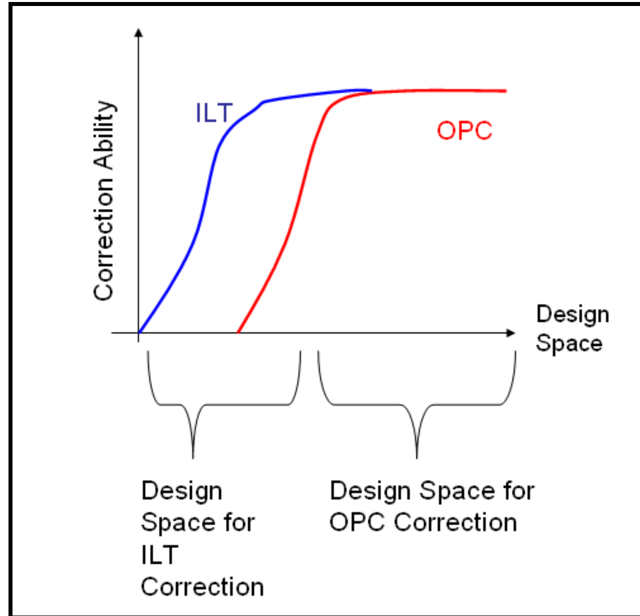

Figure 7. Design space split for localized ILT correction after OPC.

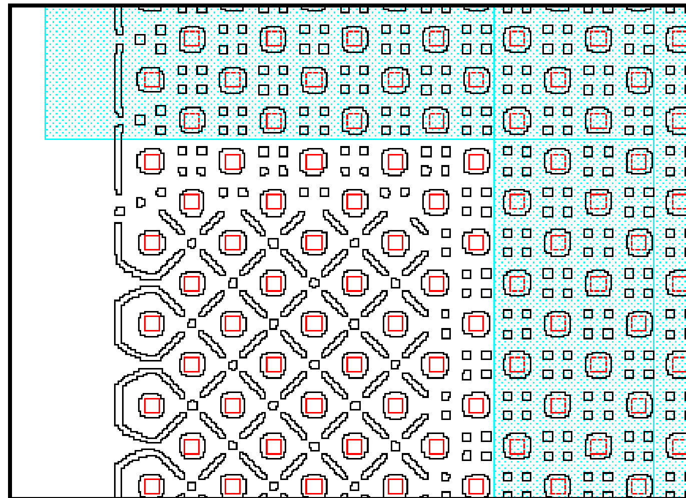

Figure 8. Hotspot ILT (HSF) applied locally to bottom left corner, shaded top and right regions are OPC correction. This demonstrates the ability of HSF to smoothly blend the ILT srafs and the OPC srafs.

4. CONCLUSION

To conclude on the current capabilities of ILT, advancements were made in the inversion methods, manufacturability, parallelization, and modeling. A localized ILT method has also been developed which has shown the ability to blend solutions which are fully solved by ILT with those fully solved by OPC. For a contact patterns mask write time reduction and margin improvement were achieved by a combination of improved automated mask segmentation control, more robust inversion algorithms, and more accurate modeling. Continued efforts to enhance the features of the ILT will made to improve the applicability of ILT to IC fabrication, most importantly in the areas of improved modeling and runtime reduction.

// 5. ACKNOWLEDGEMENTS

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