Inverse Lithography Technology (ILT) and its Latest Development
-Enabling 45nm Generation with Dry Steppers

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Biography

Dr. Linyong (Leo) Pang is currently the VP of Product Marketing and Business Development at Luminescent Technologies. Prior to joining Luminescent, Dr. Pang made his mark in semiconductor technology as the Inventor of i-Virtual Stepper while contributing to Product Marketing at Numerical Technologies, and subsequently as Product Marketing Manager in the DFM group at Synopsys. Before joining Numerical, Leo worked at Acuson Corporation, where he invented and developed medical imaging product “FreeStyle”. He also co-founded China’s first online game company (xkx.com.cn) in 2000 at his spare time. Leo has 14 issued patents, 11 pending patents, and 32 publications in fields of image processing, medical imaging, EDA, and semiconductor. He earned his Ph.D. at Stanford.

Dr. Daniel Abrams, CTO and cofounder Luminescent, Dan Abrams is a scientist and entrepreneur who founded two successful software companies prior to Luminescent. Dan has served as a Research Scientist at Caltech’s Jet Propulsion Laboratories (JPL); he earned his Ph.D. at MIT, and his bachelor’s at Stanford.

Dr. Yong Liu is Director of Marketing and Applications at Luminescent Technologies. He was previously with Third Dimension Design, Cadence Design, Numerical Technology, Synopsys and AMD, with positions as president, architect, marketing manager and R&D manager. His investment in Archer Design Technologies, as a representative of AMD at Sematech, returned 9X for member companies. His invention of general vortex mask extended Dr. Levenson’s vortex mask method to random contact holes. His interconnect parasitic capacitance formula was the first analytic formula for parasitic extraction. His current interest is in Design For Manufacturability (DFM) and interconnect parasitic extraction. Dr. Liu received his Ph.D from U.C. Berkeley.

Abstract:

Increasingly, for semiconductor manufacturers moving to advanced nodes – 90nm, 65, 45, and below – the greatest challenge is lithography. This is because lithography is fundamentally constrained by basic principles of optical physics. At 65 nm, a line is less than a third of the effective wavelength; as the industry moves forward, optical diffraction and interference are becoming fundamental obstacles, not just second order effects.

It has long been known that the best lithography that is theoretically possible can be achieved by considering the design of photomasks as an inverse problem -- and then solving the inverse problem to find the optimal photomask for a given process, using a rigorous mathematical approach. Inverse Lithography Technology (ILT) has been explored for many years[1-8]. Although these early approaches to ILT often resulted in superb lithography, they were generally impractical in a production environment. Run-times were many orders of magnitude too slow, and the resulting masks were often too complex to manufacture.

In this paper, we discuss the first ILT approach that can rapidly solve for the optimal manufacturable photomask design and is suitable for use in a production environment. We will discuss ILT principle and its latest development at Luminescent, in particular, in the areas of SRAF generation, Manhattan constraint mask, and mask rule correction (MRC). Results collected internally and from customers demonstrated that, ILT has a great potential to enable 45nm generation with dry steppers.

Data:

ILT AND ITS TECHNICAL ASPECTS

By definition, ILT means knowing the forward transformation of lithography process, how to mathematical calculate the optimized mask which

produces the desired wafer target with the best pattern fidelity and largest process window. The forward transformation is modeled accurately, which may take into account all of the elements of the transformation from mask to wafer: for example, the electromagnetics of the 3D mask, the optics of illumination and the lens, the behavior of the photoresist, the dose and focus conditions, aberrations, etc. However, the problem thus stated is ill-posed; because the forward operator f is many-to-one (that is, many different masks will yield identical on-wafer results), the function has no well-defined inverse. Moreover, for typical target patterns (e.g., a drawn layout with Manhattan geometry and sharp corners), there does not exist any mask function which will produce exact drawn wafer target. These issues are addressed by recasting the inverse problem as an optimization problem.

We define a merit function, also called a cost function, energy function, or Hamiltonian (by analogy to quantum mechanics). This function is indicative of the quality of the solution, or the "goodness" of the mask. In other words, this Hamiltonian is the absolute value of the difference between the wafer image and the target pattern, integrated over the area of the mask. In practice, a number of additional elements may be included in the Hamiltonian. For example, the wafer pattern at various conditions throughout the process window (i.e., over or under exposed and/or plus/minus focus), the NILS of the image, the robustness against MEEF, or other factors as deemed appropriate. The actual functional form may be different from the form as described above as well. Elements that are not directly related to lithography may be included; for example, simple masks may be preferred over complex masks, and terms to this effect may be included in the Hamiltonian as well. What is essential is that the Hamiltonian is a functional of the mask function, and that minimizing said Hamiltonian allows us to find the optimal mask, according to the criteria we have chosen.

Another important aspect of the minimization problem comes in the form of constraints. A variety of constraints are imposed by the realities of mask manufacturing; for example, two disjoint chrome regions must be separated by a minimum distance, and a chrome line must have a minimum thickness. We address these constraints by defining a sub-space of the full Hilbert space of mask functions, and restricting our solution to this sub-space.

A key distinctive feature of ILT is the absent of pattern-dependent heuristics, and the ability to broadly explore wide areas of solution space. ILT algorithms frequently lead to mask patterns which are unanticipated by a knowledgeable practitioner. As will be shown in the next example of the problem of placement of subresolution assist features (SRAFs), there are mask features that do not print on the wafer which are detached from the edges of the main mask patterns, and yet manipulate the light reaching the wafer so as to accentuate the wafer image. In the past, these were placed empirically, with great care, and frozen in place during the computation of the rest of the mask. In contrast, ILT can determine optimal SRAFs simultaneously with the rest of the mask. The absence of segmentation scripts is a significant advantage because it usually requires significant engineering resources to write such scripts for different patterns on different design layers.

Figure 1 shows an example to demonstrate the power and flexibility of ILT[9]. The goal is to print a regular contact array with 110nm CD, 440nm pitch. The numerical aperture of the stepper is 0.78, the illumination source is a disk with a sigma of 0.3. In Figure 1 we show a continuous tone mask, an attenuated phase-shifting mask without mask constraints, and an attenuated phase-shifting mask with Manhattan constraints, all designed with ILT, to print the above described contact hole array. The process window of images produced by the Manhattan attenuated phase-shifting mask is 574 nm DOF at 7% exposure latitude. The aerial image contrast is 0.85, well above 0.35, which as a rule-of-thumb is the minimum aerial image contrast required to print on wafer. It is quite remarkable that the combination of a single small central region, with four distinct surrounding lobes, should optimally print the contact pattern. Such remarkable patterns illustrate the power of ILT, which finds solutions that are often unexpected. Notice also the assist features found further from the contact, around the perimeter of the image.

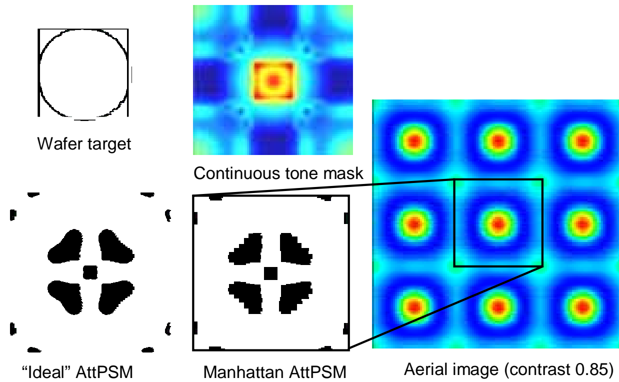
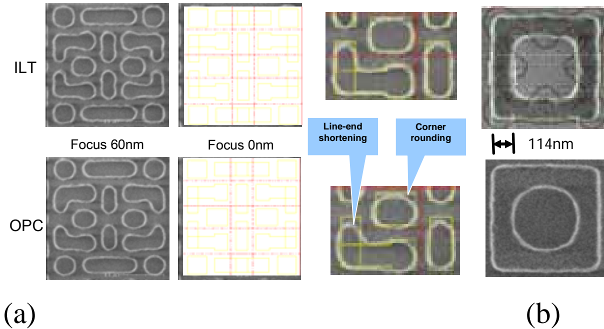


Figure 1. ILT contact array example: contact target of 110nm CD, 440nm pitch. Three types of masks were generated from ILT: continuous tone mask, "ideal" attenuated phase-shifting mask, attenuated phase-shifting mask with Manhattan constraints, and the aerial image simulated using Manhattan AttPSM.

By finding the optimal mask patterns, ILT brings an additional benefit of improved wafer pattern fidelity and process window. It also opens the possibility of using existing lithography equipments (e.g., scanner) into smaller geometries; in other words, extending the life of existing lithography equipments. Since every pixel is considered in the computation; in a pixel-based ILT implementation, the side-lob-printing problem which had become a headache for edge-based OPC due to its fundamental edge-sampling-based approach, is easily eliminated. The following three examples demonstrate such benefits.

Figure 2 shows some examples of wafer prints using ILT masks. The result on the left (Figure 2(a)) is from a 65nm metal 1 layer[10]. In this case, both ILT and OPC used optical model. Two images for both ILT and OPC were captured at best focus, and at plus 60nm defocus. It shows wafer image using ILT mask has a better pattern fidelity through process window. From the zoomed-in pictures (insets at right), it is clear that ILT produces less line-end shortening and corner rounding issues. The result on the right (Figure 2(b)) is from another test mask and test wafer[11]. The design target is a square "donut" shape with very small dimension (CD 114nm on wafer). From the inner shape of the "donut" it is clear ILT can resolve smaller features better than OPC in this case.



(a) (b)

Figure 2. ILT and OPC wafer images. (a). Through focus wafer patterns of metal 1 layer, where outline is the design target. The insets at right are a magnification of a selected portion of the 0nm focus condition. (b). a square "donut" shape (CD 114nm on wafer).

Using modern numerical methods and the latest processors, it is now possible to quickly solve the resulting minimization problem. Our implementation divides a large photomask into small regions called “work units”. These are distributed to a cluster of compute nodes, which can then process many work units in parallel. The solutions are then stitched together to form a complete mask. A large number of real full-chip designs have been processed this way through our software. The results can thereby be obtained quite quickly. In one recent example, a large 4cm2 die (wafer scale) was processed overnight.

THE LATEST DEVELOPMENT OF ILT

SRAF GENERATION

SRAF is commonly used in RET. There are three major problems in the current SRAF generation: 1). Most of SRAF placements are rule-based, and such role are created using simple regular patterns, such as line/space, or contact with different pitches. Such rule might not applicable nor accuracy for complicated geometries in the real design; 2). SRAF and OPC are two separated process – first generate SRAF, then run OPC. This is time consuming. 3). OPC only applies to main pattern. SRAF cannot be optimized during OPC any more.

In ILT, SRAF is automatically generated during the inversion calculation, and they are optimized simultaneously with main features. Therefore, the

SRAF generation becomes a straight forward, single step process[12].

To illustrate the adaptive properties of this implementation of inverse lithography in one dimension, a series of regular one dimensional gratings with varying pitch is used with realistic design and lithographic parameters. Figure 3 shows a selection of 70 nm darkfield gratings, varying in pitch from 210nm to 800nm.

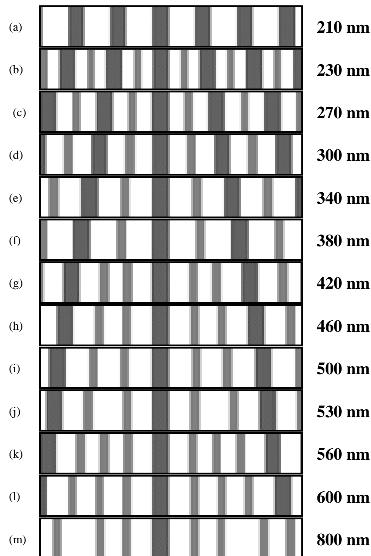


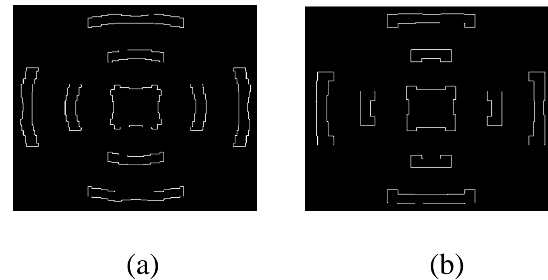
Figure.3. Simultaneous mask creation and SRAF placement using ILT for regular gratings. As the pitch of the 70nm grating elements is varied from 210nm to 800nm, (a)-(m), the number, position, and width of inter-feature SRAFs is adjusted automatically.

As shown in this example, the simultaneous creation of mask elements overlying the design features and assist figures distinct from design features has four notable properties within the scope of this study. First, the assist features are added as the pitch increases. Compare, for example, Figures 3a and 3b, 3f and 3g, and 3j and 3k. Second, the spacing between assist features grows for increasing pitch but fixed numbers of assist features (Fig 3b-3f, for example). Third, the assist feature size changes for increasing pitch but fixed numbers of assist features, e.g., in Figs. 3b-3c. Fourth, the “main” mask features, that is, the mask elements overlying the original design features also change in width for increasing pitch but fixed numbers of assist features (compare Figs. 3a and 3b, for example).

MANHANTTON CONSTRAINT MASK AND PROGRESSIVE MRC IN INVERSION

The number 1 issue that prevent ILT mask to be used in production is mask complexity. In the previous ILT implementation, the mask constraints were not considered, therefore, generate mask with curved geometry and many small fragments, which makes the mask writing, inspection, metrology, and repair very challenge.

In Luminiescent’s ILT approach, the mask constraints are first time built into the inversion solver. User can specify mask rules, such as minimum CD, minimum space, minimum area, and minimum fragment length on the Manhattan shaped mask[13].



(a) (b)

Figure 4. ILT mask patterns for isolated contact with different user specified mask rules: (a). min. fragment length 20nm, min. CD/space 25nm; (b). (a). min. fragment length 20nm, min. CD/space 50nm .

As shown in Figure 4, user can specify different mask rules, in this case, the minimum fragment length 20nm in 4a, 50nm in 4b, and minimum CD and space both 25nm at wafer scale. ILT program will generate different optimized patterns respectively based on those user specified settings.

A progressive mask rule correction (MRC) is also implemented in ILT. During the inversion calculation, mask rules, especially minimum CD, space, and area are checked. If a violation happens, then a correction, which amount is based on local MEEF, will be applied during the inversion. This guarantees the mask patterns from ILT satisfy mask house’s mask rules.

ILT ENABLING 45NM WITH DRY STEPPERS

Recently more and more customer tape-out shows consistent evidence that ILT could enable

the 45nm generation with dry steppers instead of going with immersion steppers.

One of the common myths that ILT cannot change the basic resolution physics, therefore, cannot improve the fundamental resolution. This is not correct. Firstly, the resolution is determined by how many order of diffractions that a pattern can receive through the stepper optical system. If only zero order diffraction is received at the wafer image plane, then you would only see a constant background, in other words, the pattern cannot resolved. That's the fundamental limitation of resolution. There are two common practices to increase the number of diffractions at the wafer image plane: using OAI or using phase shift mask. The reason of such two approaches were extensively explored in the last two decade is because the computation required is manageable by human beings. However, there is a third approach which is less popular and only be explored recently – using the interaction of diffraction on mask patterns. SRAF can be considered as the first try in this approach for simple isolated line patterns. To make this approach applicable to complicated random patterns on the real chip designs, it is only possible when a fast inversion lithography computation engine is developed; secondly, for each generation, the resolution is actually not limited by the dense line/space patterns, because usually regular dense/line space patterns can get the largest number of diffractions from neighbor patterns; In reality it is the line-end and other features limits the lithography capability. For example, in the DRAM core, resolving the line/space is not an issue; the issue is how to break line/space into small segments. ILT can help in such case, because it requires a sophisticated consideration of shapes in surrounding area to increase the order of diffractions; thirdly, the K1 factor that foundry feels comfortable to use is usually larger than 0.38, which is high; Such K1 factor is calculated from dense line/space pattern. The reason it requires such high K1 factor is because the other geometries, such as line/end, has smaller K1 factor, and foundries have to consider all types of geometries to be safe. ILT is the only way to increase the diffraction order for random geometries. With ILT, the lithography capability can be extended to its largest possible.

We have seen ILT is able to improve the DOF of the most challenge contact layer in a 45nm DRAM core from 240nm, which is barely acceptable for manufacturing, and requires NA 0.92 and C-Quad illumination, to 410nm, which is very comfortable for manufacturing, and only requires NA 0.82 and annular illumination. Another example is that ILT enables 45nm SRAM critical layers (poly, diffusion) with single exposure, NA 0.92, annular illumination. All of such evidence on simulation and wafer shows a huge impact of ILT to the semiconductor industry – 45nm lithography with dry stepper.

Conclusion:

In this paper, we briefly described the frame-work formulation of ILT with some specifies of the implementation of ILT by Luminescent Technologies, and presented the latest development of ILT, in particularly, SRAF generation, Manhattan constrained mask and progressive MRC during inversion. We have demonstrated a variety of results using ILT and dry stepper to print 45nm critical layer patterns.

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