Hotspot Fixing Using ILT

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ABSTRACT

For low k1 lithography the resolution of critical patterns on large designs can require advanced resolution enhancement techniques for masks including scattering bars, complicated mask edge segmentation and placement, etc. Often only a portion of a large layout will need this sophisticated mask design (the hotspot), with the remainder of layout being relatively simple for OPC methods to correct. In this paper we show how inverse lithography technology (ILT) can be used to correct selected regions of a large design after standard OPC has been used to correct the simple portions of the layout.

The hotspot approach allows a computationally intensive ILT to be used in a limited way to correct the most difficult portions of a design. We will discuss the most important issues such as: model matching between ILT and OPC corrections; transition region corrections near the ILT and OPC boundary region; mask complexity; total combined runtime. We will show both simulated and actual wafer lithographic improvements in the hotspot regions.

Keywords: ILT, OPC, Hotspot, model matching

1. INTRODUCTION

In the regime of shrinking k1 factors with fixed scanner resolution, it is becoming more difficult to produce yielding chips. Without a clear path the next generation of scanners with either reduced lambda or higher NA that can increase resolution, more and more burden is being placed on techniques to solve yield problems. While source optimization can help solve some problems, it introduces more problems in other areas (such as OPC). Also, as the design size shrinks and the optics remain fixed, the effective interaction between design features becomes larger, meaning that design rule decks become more complicated and may miss some critical areas which can later become hotspots.

In this paper we discuss a new method of applying ILT to specific hotspot region, which allows the user to get the improved process margin that ILT gives without the overhead of performing expensive computational solutions on the entire chip.

Prior work in this area has been focused in a few different areas. One main area is DFM hotspot fixing which aims to modify the design when a lithographic hotspot is found[1,2]. This approach requires close feedback between the design and RET teams which is not always feasible, and it also may not be physically possible to modify a design and achieve the same chip performance. The approach we take is more in line with methods that address the hotspot within the OPC flow. Some prior methods have studied using specialized OPC within a specific hotspot region[3,4]. Another has attempted to copy portions of SRAFs found in the hotspot region by using computational lithography and use them to replace rule generated SRAFs[5]. Our method goes a step further and truly uses full ILT within the hotspot region, employing a mask blending method at the boundary so that features both inside and adjacent to the hotspot region are monitored during the mask optimization process.

The outline of this paper will be to first discuss the ILT HSF algorithm, including the setup and model issues. After that we will show some simulated results, and finally taped out wafer results.

2. HOTSPOT FLOW

2.1 Outline of Flow

This section discusses the outline of the ILT HSF flow, including setup and model issues. The basic outline of the ILT HSF flow is as is shown in Figure 1.

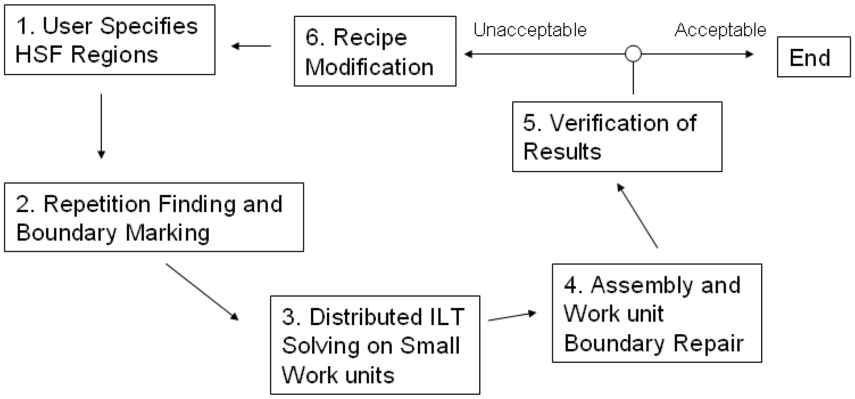

Figure 1. ILT HSF flow.

The creation of a model can be done at different points in the flow depending on the use type. If the input mask has been created using ILT itself, then no model recalibration may be needed, however, it is possible that the “hotspot” to be repaired is actually a problem because of model error and a recalibrated model could be used in the HSF region to obtain better wafer matching there. Model calibration can occur either prior to step 1, between steps 1 and 2, or possibly during step 6. The details will be discussed in section 2.2.

2.2 Model Calibration

In order to use masks from two different tools which will be contiguous it is necessary to have the models match as closely as possible to each other (and of course to the measured wafer data). Depending on the size and variation of the patterns in the HSF region we can choose from one of the methods in Table 1.

Model Calibration Approaches

Design Type	Calibration Method
1. Varied, random	Use wafer data, or OPC simulated data
2. Repetitive, nonrandom	Use wafer data, then fine tune with subset

Table 1. Model calibration approaches for HSF

In general if the HSF region is very large and contains a wide variety of patterns it may be better to use ILT for the full layout instead of correcting with HSF. However, it is still possible to fit a model to true wafer data and then use it. In practice if the data is clean enough we have seen that this method works acceptably with minimal mask size dimensions between ILT and OPC at the HSF boundary. If the models do not match well from this method it is possible to make a simulated data set which can include all important patterns and many dose/defocus/bias FEM points. This requires more user work to set up but can generate a noise free data set.

In practice the method which has worked acceptably well is a hybrid approach which is to first fit a model on the wafer data set and then fine tune the model with a subset of this set using simulated images to ensure image contour matching in the HSF region. An example of this is to use a single critical anchor pattern and adjust the resist threshold value in the model so that the ILT and OPC models match for nominal imaging conditions at that point. This is a quick method which has worked well in practice.

2.3 Mask Blending at HSF Region Boundary

The blending of the ILT and OPC masks at the boundary of the HSF region is an issue that must be handled even if the models used in ILT and OPC are identical. Firstly, there is an assumption that outside of the HSF region the OPC mask has produced a result that is acceptable to the user. Then, from the HSF region boundary there are a number of concentric regions on which different ILT algorithms will be run. The general idea is that as you move farther from the boundary, more aggressive correction can be done.

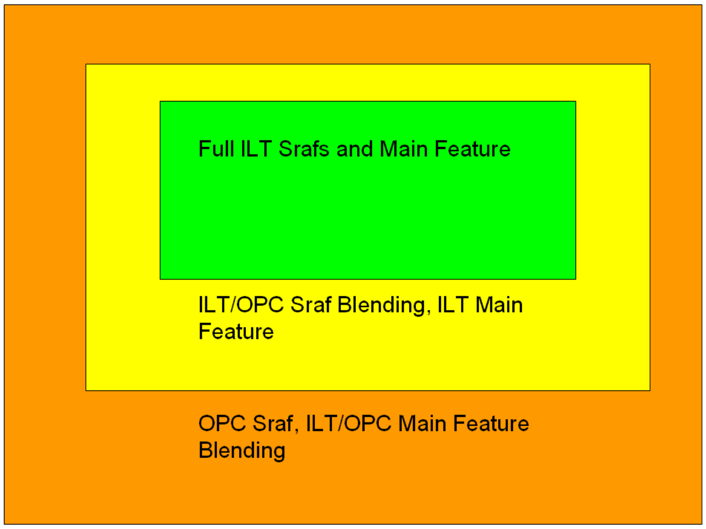

Figure 2. Concentric HSF regions showing where different algorithms will be performed. Orange: outermost region where least aggressive correction is done. Yellow: middle region where SRAF blending is done. Green: core region where full ILT is performed.

Figure 2 shows a schematic of the blending regions. The most critical is the middle region where SRAFs must be blended. In this region various geometric and inversion methods must be used to handle SRAF-SRAF conflicts when the ILT SRAFs and OPC SRAFs are in close proximity to each other. Ultimately we are heavily reliant on the inversion algorithms to be able to automatically adjust the mask appropriately so as to achieve the best lithographic results given both the MRC constraints and boundary conditions of fixed OPC SRAFs in the outermost concentric region. At the outermost edge of the HSF there are only small corrections made to ensure that MRC is acceptable.

3. SIMULATED RESULTS

Before getting into the application of the HSF to the real mask patterns (used in recent sub-20nm manufacture), which will be shown in Section 4, let us first provide the result of the application of the HSF to the typical test patterns. Here, we have tested two types of mask patterns. One is the pattern that was corrected by a conventional OPC tool, and the other is the one optimized by ILT, both of which are the cases we can meet in the application of the HSF to real mask optimization process.

3.1 ILT HSF Applied to OPC Input Mask

First, let us show the case that the HSF has been applied to the OPC mask. The test pattern is composed of contact holes with varying pitch. The intended hot spot is the region where the pitch is varying rapidly, as depicted in Figure 3. In the figure, HSF region and blending region are indicated with boxes colored in blue and red, respectively. Note, in the HSF area, the ILT main features and SRAFs (blue) have various and more complicated shapes, while the OPC polygons including SRAFs are simple tetragons. This implies the ILT patterns in the HSF region is more optimal solution than OPC patterns, which yields wafer images that have better EPEs and PV band. Indeed, as shown in Figure 4, the simulation contours (green) of ILT solution are closer to the target (red) and have smaller bands than those of the OPC solution. The contours are the images under various process variations such as dose, focus, and mask bias. The detailed simulation results are shown in Table 2, which shows the enhancement of PV band, MEEF and NILS in the HSF region and blending region.

Region	PV band (nm)	MEEF (nm)	NILS
HSF	3.67	0.92	2.92
Blending	5.46	2.22	2.81
OPC	5.98	2.33	1.60

Table 2. PV band, MEEF, and NILS evaluated in HSF, blending, and OPC region.

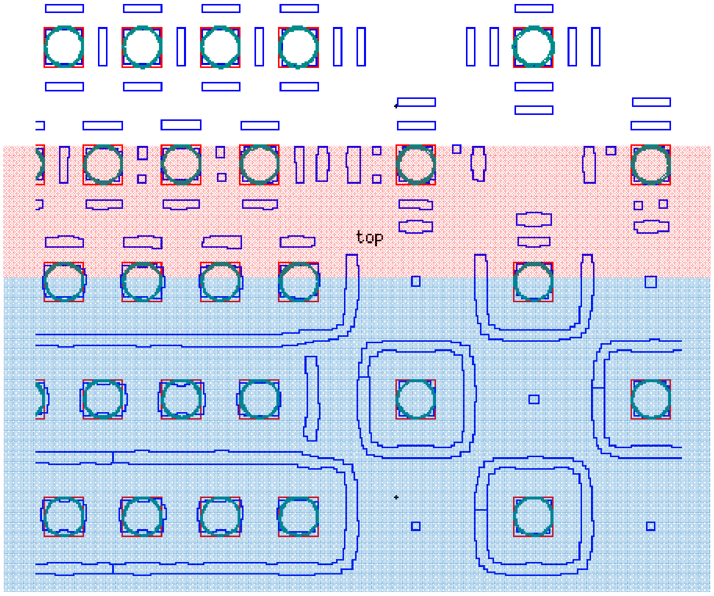

Figure 3. HSF applied to OPC mask. HSF region (blue) shows complete ILT solution and blending region (red) shows the smooth transform to OPC mask to ILT mask.

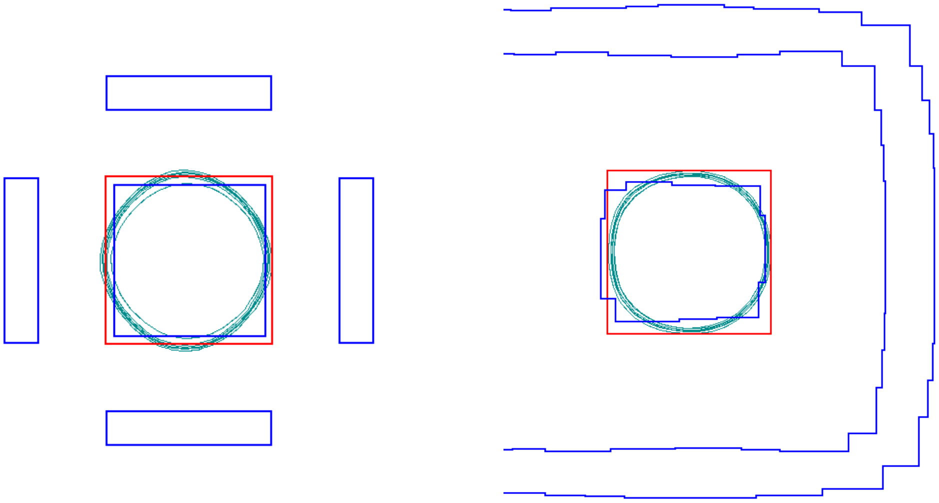

Figure 4. OPC polygons (left) and ILT polygons (right, in HSF region) and their image contours.

3.2 Aggressive ILT HSF Applied to Simple ILT Input Mask

In this section we show an example where the input mask is a simple ILT mask and within the HSF region a more aggressive ILT solution is found by putting more emphasis on off nominal images in the inversion cost function. Figure 5 and 6 shows the change of mask patterns after the application of HSF. The simulation result is similar to the case of HSF applied to OPC mask which has been shown above. We see the enhancement of PV bands in the HSF region, as depicted in Figure 6, where we can see that the PV band is decreased in the HSF region, and the mask is blended well across the boundary.

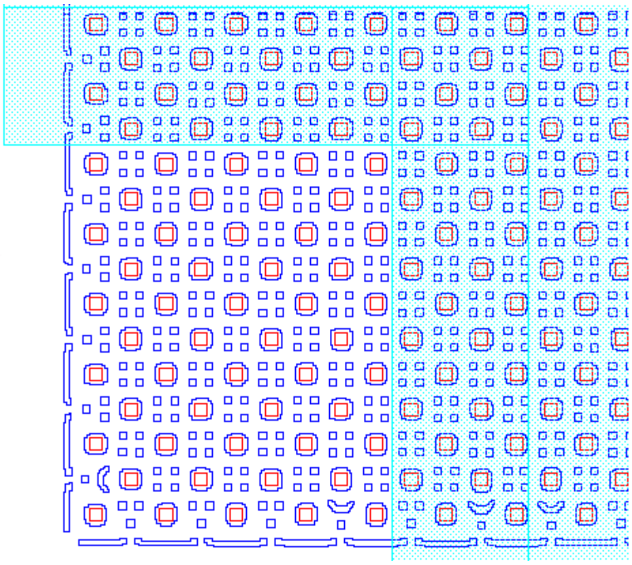

Figure 5. Target design (red), input simple ILT mask (blue), fixed region (region shaded light blue), HSF correction region (unshaded region).

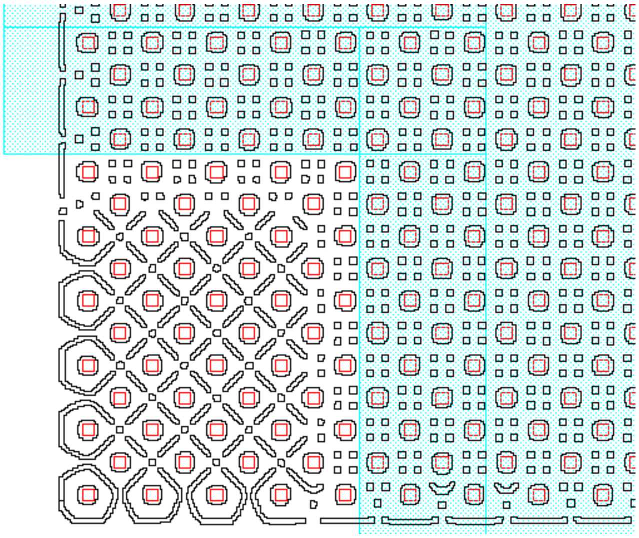

Figure 6. Target design (red), final post-HSF blended mask (black), fixed region (region shaded light blue), HSF correction region (unshaded region).

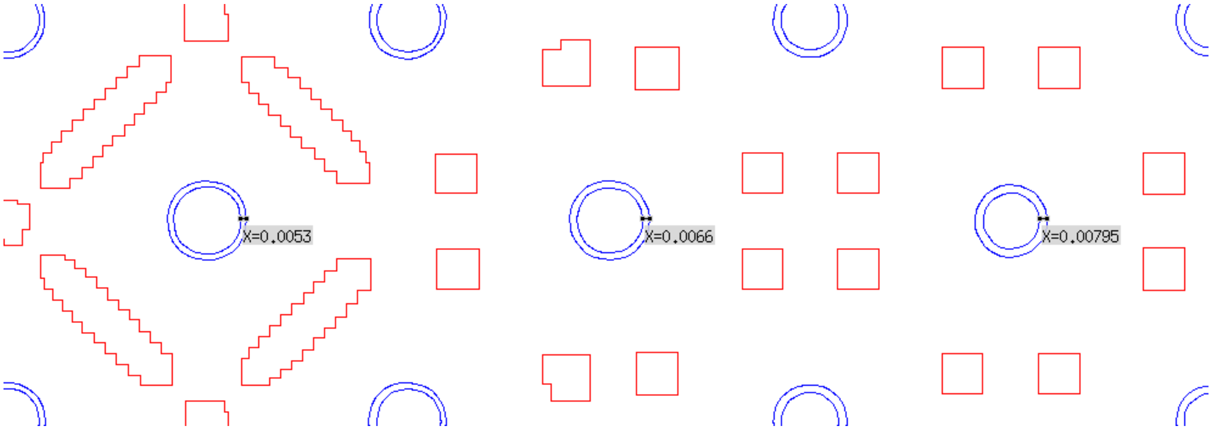

Figure 7. Nominal and defocus images (blue) and SRAFs (red) across HSF region boundary. Left side is aggressive ILT HSF repaired mask, middle is blended mask, right side is input simple ILT mask. PV bands from left to right are 5.3nm, 6.6nm, 7.95nm.

4. WAFER RESULTS

Now, as advertised, we present the result of HSF applied to patterns in real manufacture. The targeted one is the OPC mask obtained from the dense contact-hole pattern whose minimum pitch is around 100nm. The pattern under consideration includes not only simple tetragons, but also the polygons having more than 4 edges with large jogs. Moreover, the polygons are not aligned and, due to the small pitch in both of the horizontal and vertical directions, the distances between the corners of polygons are as small as MRC limit. Hence, the resulting OPC mask does not yield good wafer images, including large nominal EPEs and PV bands. Especially, the small corner to corner distance together with MRC limit make it hard for the OPC to find the optimal solution, since the conventional fragmentation of OPC cannot deform the polygon edges freely enough to match the restrictions by MRC.

Therefore, the application of HSF to such patterns was natural to get enhanced wafer image, and the final result is inspiring. Although we cannot show the real wafer image obtained by HSF, the numerical data in Table 3 evidently shows the enhancement of PV bands and MEEF in addition to EPE.

Tool	Region	EPE (nm)	PV band (nm)	MEEF
HSF	Center region	0.05	3.17	2.45
	Blending region	1.17	7.00	2.66
	Complicated Polygon	0.71	1.95	1.21
OPC	Center region	2.14	3.68	2.94
	Blending region	3.57	7.71	3.26
	Complicated Polygon	3.77	2.11	1.56

Table 3. EPE, PV band, and MEEF of HSF patterns and OPC patterns

5. CONCLUSION

As semiconductor fabrication goes into sub-20nm era, the optimization of full-chip mask design by conventional proximity correction is now at the breaking point in achieving proper process margin and stable manufacturability. The inverse lithography technology (ILT) is one of the strong solutions to overcome the limit, since it finds the optimal solution of the mask in a natural manner that the polygons including assist features are deformed freely changing their topologies in the aid of level-set function.

Despite such a superb property of ILT in achieving enhanced mask design, it has one weak point that it takes more time to get the final solution compared to conventional OPC. One idea is to resolve this problem is to apply ILT to the small regions of the mask design corrected by OPC that include hot spots where the patterns have large PV bands or bad NILS, which has been realized through the HSF using the inversion engine of ILT.

In this reports we have applied the HSF to various cases including OPC test mask, ILT test mask, and OPC real mask in current manufacture. For all the cases the images in the HSF region as well as in the blending region have shown better qualities in terms of PV bands and NILS. Moreover, in the application of HSF, the matching between the ILT model and OPC model has been done successfully.

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