Exploring the impact of mask making constraints on double patterning design rules

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ABSTRACT

In order to achieve an economical design-to-mask (DTM) development cycle in the low k1 domain, designers, lithographers, and mask makers needed to move away from many sequentially isolated developmental activities onto one collaborative environment managed by a computational lithography platform that integrates their respective ecosystems. [1,2] A successful development cycle used to be achievable by designers providing designs to lithographers, who then provided RET/OPC solutions to realize designs, but once k1 fell below a certain level, the lithographers could not provide solutions to realize some critical designs, which then required feedback to designers for further redesigns requiring further lithographic evaluation cycles. So collaboration and automations between lithographers and designers became necessary to reduce feedback loops and development cycle time. RET and design solutions also were impacted by mask making, and so mask maker's feedback on MRC and other constraints needed to be integrated for all three groups to achieve an economical DTM.

As many lithographers attempted to print sub-80 nm pitches with 193 nm wavelength, it became necessary to use double patterning to achieve feature resolution. With the effective pitch doubling on each split layer, there could be significant increased design rule freedom for certain complex design situations. Using an integrated computational lithographic platform, one could find design space sweet spots that could further achieve optimal lithographic performance. In this paper, the optimization of design rules (DRD) for double pattern designs (~60 nm pitch) was explored with the mask maker's perspective. The experiment to be presented started with a 2x nm design set of clips. Each set of clips underwent size/width/space/pitch variations to generate a design space, and then each design space underwent SMO with an inverse lithography technology (ILT) engine using various mask MRC's and manhattan segmentations. The lithographic results were analyzed with respect to MRC and manhattan segmentation to show their impact on design space and mask solutions.

Keywords: ILT, Inverse Lithography, SMO, Source-mask optimization, OPC, MRC, Design Rule Development

1. INTRODUCTION

As pitch continues to scale below resolution limit and complexity in design increase, designers required more OPC/litho/mask feedback to avert lithographic failures and maximize design space fulfillment in their provided designs. The number of feedback iterations also increased with the need for designs to comprehend different domain capabilities, and so it became necessary to increase the feedback speed to maintain reasonable DTM's. Design rule development in conjunction with ILT source mask optimization (DRD-SMO) was developed as a platform to allow user to gauge and optimize lithographic performance for a design space taking into account parameter changes that can occur in three different functional domains (design, OPC/litho, and mask fabrication).[3,4] The ability to adjust different domain parameters and evaluate lithographic performance established the core abilities of this tool.

DRD-SMO flow typically began with a set of designs that were varied to generate a design space representative of all designs that could be laid out in a full-chip tape out. By taking the design space through the DRD-SMO process flow described in Figure 1, user could determine the lithographic viability across it. In addition to running this flow with a fixed setup of source and/or inverse lithography technology (ILT) recipe, it also could optimize for source and mask solutions (SMO) on a subset of the design to determine optimal illuminator that would then be suitable to the entire design space. This provided an optimized solution tailored to input designs. After mask solutions were obtained, lithographic qualities were assessed to determine design space fulfillment. Changes to any functional domain parameters from design rules to lithographic process model (resist & optics parameters) to mask making could be further optimized to improve design space fulfillment.

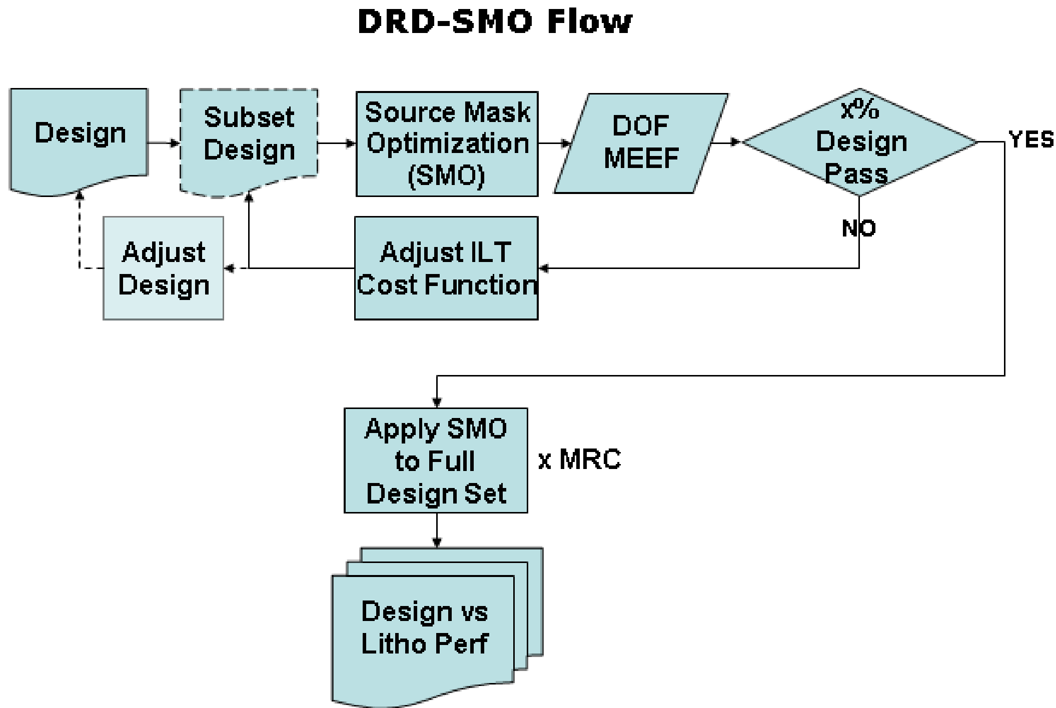


Figure 1. DRD-SMO flow.

As a test case that is pertinent to a photomask conference, this paper assessed the lithographic impact of various MRC constraints on a design space that comprised of BEOL, 60 nm pitch, routing layer designs. From a set of 490 different design variations, an optimal source mask solution was found using DRD-SMO. Subsequent inverse lithography technology (ILT) results with this solution showed that lithographic performance failure, especially MEEF, was driven by two specific design rules. The modulation of MRC mask parameters was then shown to be a means to avoid a good portion of these MEEF-related failures leading to an expanded design space fulfillment.

2. EXPERIMENTAL

2.1 BEOL Metal Routing Design Inputs

The designs selected for this paper were composed of 10 different routing patterns that have four design rules which had been shown statistically to cover 98% of all typical auto-routed structures for 45 nm BEOL metal layers.[3,4] Elements of these design rules had been prevalently found in other published articles.[5,6,7,8] Figure 2 showed these patterns along with their four fundamental design rules. The variations over these design rules created a design space for the conducted DRD-SMO experiments. Of the 490 different design combinations, the design variations included: LE-LE space from 32-75 nm, wire length from 216-240 nm, route width from 65-90 nm, and LE route space from 48-75 nm. The final silicon pitch for these patterns was 60 nm with a 30 nm width. At this pitch double patterning process became a requirement, and the assumed process was litho-etch-litho-etch (LELE) with 10 nm etch bias. After splitting into two layers the pitch of each decomposed layer was 120 nm. The 30 nm lines with 90 nm space were biased to 40 nm lines with 80 nm spaces. A Luminescent splitting routine produced the various litho target splits as shown in Figure 3. The splits in these experiments had 30 nm of overlap at the cut regions between layers, which was been shown in simulation to have good lithographic margins.

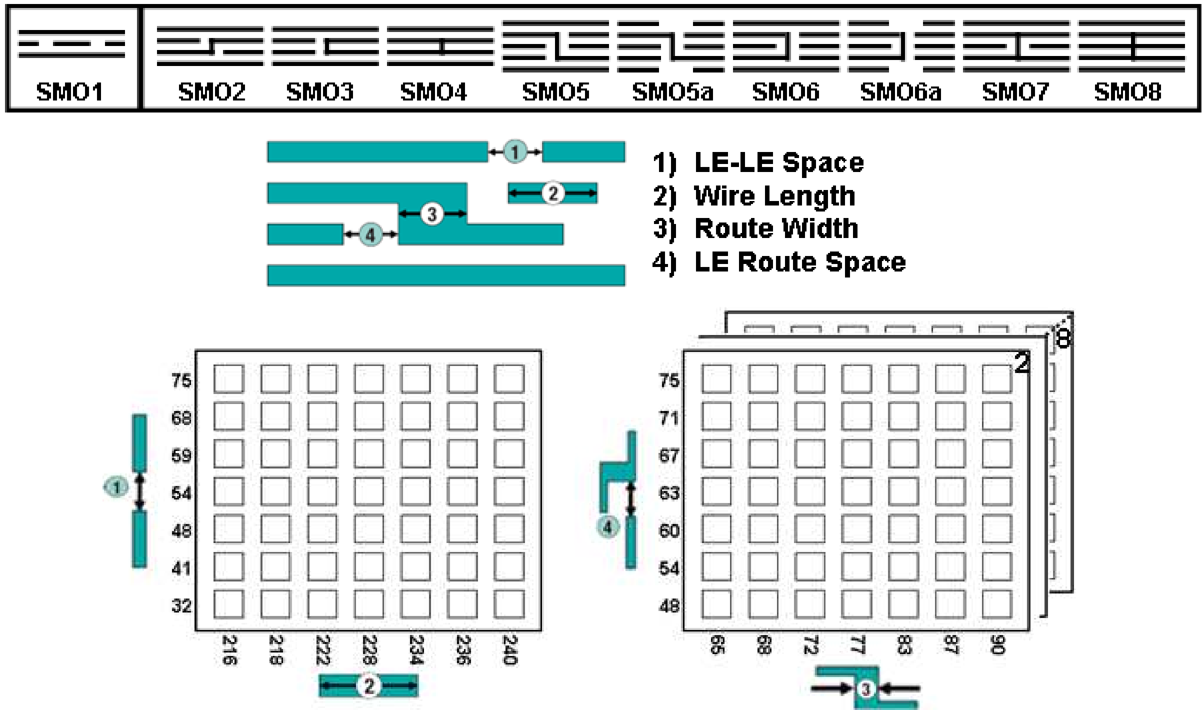


Figure 2. Ten routing designs along with their variations of four fundamental design rules are used to generate the design space for DRD-SMO .

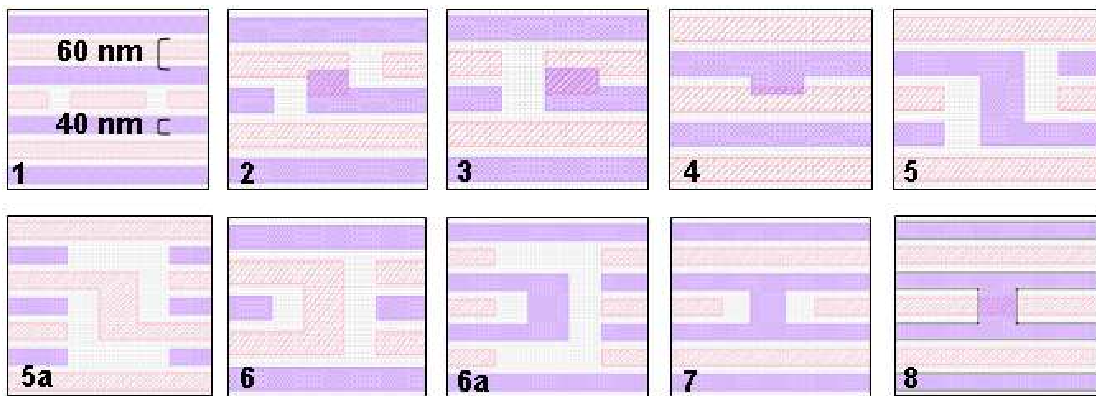


Figure 3. Ten routing designs are decomposed into two separate target layers for LELE.

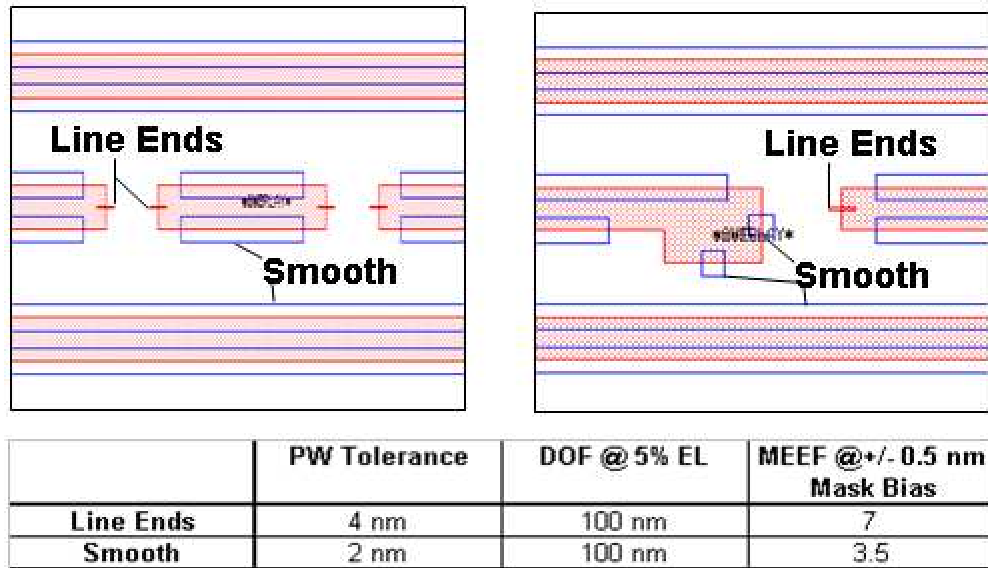
2.2 Lithographic Process Parameters & Requirements

All ILT solution and simulation results were conducted with Inverse Explorer™ system with the following settings:

NA = 1.35 water immersion with X-Y polarization
Tone = Dark Field
Mask = COG
Resist Threshold = 0.2
Resist Blur Sigma = 7 nm
Resist matched substrate, no reflection at resist/substrate interface

The optical and mask conditions were chosen to best suit the typical metal layer and design. These experiments were performed without any calibrated resist model, and the threshold and resist blurring amount had been chosen to best reflect a reasonable exposure condition along with a typical acid diffusion amount.

The pass/fail lithographic process requirements for each design could be seen in Figure 4. MEEF and depth of focus (DOF) for line ends and smooth were the main metric for assessing lithographic performance. DOF was calculated based an elliptical fitting inside the process window. The center on the ellipse was constrained at nominal condition (100% exposure with 0 nm defocus) with +/- 5% exposure latitude, while the defocus component of the ellipse can span out to the maximum defocus amount in the process window.



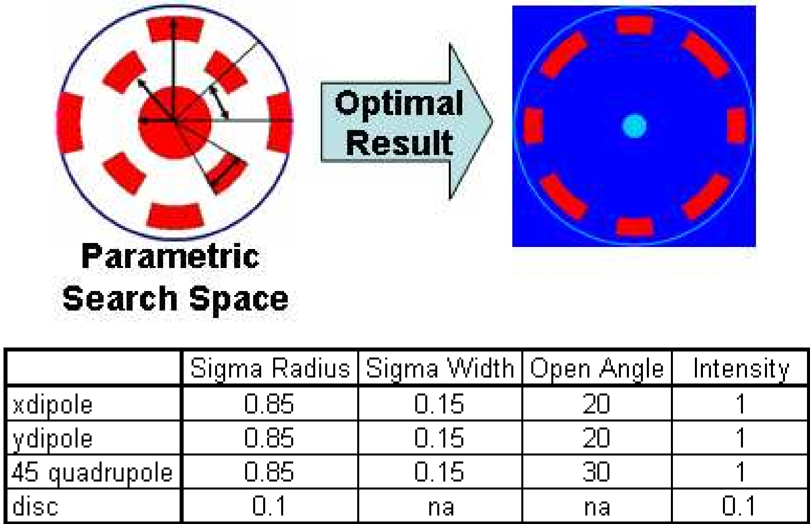
	PW Tolerance	DOF @ 5% EL	MEEF @+/- 0.5 nm Mask Bias
Line Ends	4 nm	100 nm	7
Smooth	2 nm	100 nm	3.5

Figure 4. For each decomposed designed targets, topological regions of Line Ends and Smooth are defined as depicted in the images. The DOF & MEEF requirements for each topological regions are displayed in above table.

2.3 Source Optimization

The illuminator space that was searched to arrive at an optimum illuminator for this design set consisted of superposition of x-dipole, y-dipole, quadrupole sections of an annulus, and a center disc.[10] Each parametric source component had several parameters that could be varied including sigma radius, sigma width, fan open angle, and intensity. Constraints on the parameters confined the illuminators to the pupil and forced it to maintain reflection symmetry about the x and y axes. Although this particular design set had only reflection symmetry about the x-axes, it was possible in tape-out for this design to be rotated 90 degrees. Therefore the x and y reflection symmetry was enforced during the search.

A multi-level design-of-experiment (DOE) search was conducted over a coarse set of sigma radius values for 14 different initial source combinations by turning on/off some of the superimposed illuminators components, and then followed by a finer sigma radius, sigma width, fan open angle, and intensity search on the top 2 illuminator combinations found from the coarse search. For each illuminator, ILT with the single cost function mentioned in subsequent section was conducted over a subset of 12-30 design clips from the total of 490 design combinations. The judgment for illuminator selection and search direction was based on lithographic performances and cost function values of masks produced by ILT with each illuminator. Once a post-fine search illuminator was selected, the source and ILT solution was applied to the entire 490 design combinations, whose masks were then simulated to determine lithographic viability for the design space. The optimum illuminator found with this method for this design set was a bulls-eye octopole (Figure 6).



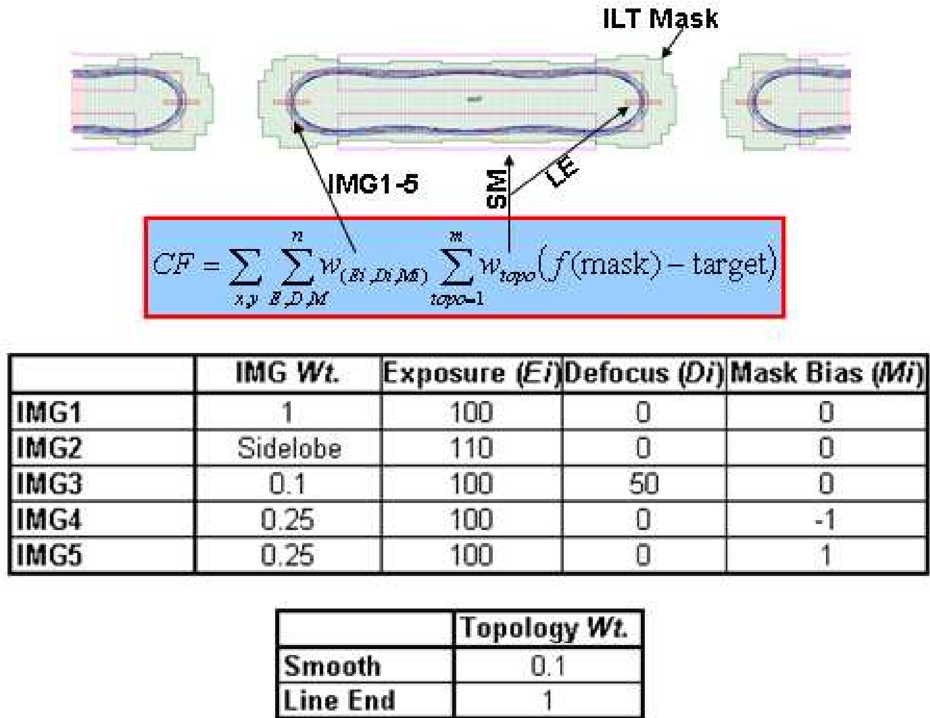
	Sigma Radius	Sigma Width	Open Angle	Intensity
xdipole	0.85	0.15	20	1
ydipole	0.85	0.15	20	1
45 quadrupole	0.85	0.15	30	1
disc	0.1	na	na	0.1

Figure 6. A search over a set of parameter space for the superposition of 4 different source types yielded a bulls-eye octopole as the optimum illuminator the BEOL route design space.

2.4 ILT Mask Inversion

During the DRD-SMO process flow, each design clip underwent ILT to create an optimal mask solution for the given illuminator. Each pair of decomposed mask solutions were subsequently simulated to determine MEEF and DOF performance. Both mask's lithographic performances had to pass the requirements specified in Figure 3 for that design clip to be deemed lithographically viable. In total ILT was conducted on 980 clips (490 pairs of decomposed targets) in this defined space.

Each ILT optimization was based on a cost function that sought to optimize a mask so that the images from such mask met some edge placement error (EPE) relative to specific topology on target edges.[9] The mathematical representation for the cost function used in these experiments (Figure 5) contained 5 anchor imaging conditions over 2 topological regions. The nominal image (IMG1) had the highest weight of 1, and indicated that the cost function would give highest priority to solving mask to achieve this image condition. Lower weight (0.1) was given to a defocus image (IMG3), while relatively higher weight (0.25) was assigned to +/- 1 nm mask biased images (IMG4 & IMG5). As for topological weights, more weighting emphasis was assigned to line ends rather than smooth. These weighting assignments were chosen as such to optimize for mask solution that reduced MEEF at line ends. As will be shown the results, depth of focus (DOF) and cost function convergence on smooth regions were not problematic with this design set especially at a relatively loose pitch of 120 nm for double patterning, and so the weighting scheme was chosen to de-emphasize these in favor of MEEF improvements for line ends.



$$CF = \sum_{x,y} \sum_{E,D,M}^{n} w_{(Ei,Di,Mi)} \sum_{topo=1}^{m} w_{topo}\left(f(\text{mask}) - \text{target}\right)$$

	IMG *Wt.*	Exposure (*Ei*)	Defocus (*Di*)	Mask Bias (*Mi*)
IMG1	1	100	0	0
IMG2	Sidelobe	110	0	0
IMG3	0.1	100	50	0
IMG4	0.25	100	0	-1
IMG5	0.25	100	0	1

	Topology *Wt.*
Smooth	0.1
Line End	1

Figure 5. ILT cost function sought to optimize a mask that could achieve balance weighting of EPE for defined anchor images (IMG#) over various topological regions. The cost function setting above was meant to emphasize improvements in MEEF on line-ends.

The process flow as described in the introduction was conducted with 3 different MRC's (26, 20, & 14 nm 1X wafer scale) applied to the mask solution to study the impact of MRC on design rules. Along with the different MRC's, a proportionate reduction in edge segment lengths was also applied to the mask solution.

3. RESULTS

Once an optimum illuminator and cost function setup were determined, mask solutions along with their lithographic measurements were collected and analyzed for each design combination. Each lithographic metric of MEEF and DOF was evaluated over the two different design rule spaces. Each design rule space plot showed a matrix of color boxes representing a combination of design rules. Color scale in the boxes were normalized to the specification of the lithography metric of interest as described in the equations in Figure 7. A normalized metric ≤1 meant that particular design combination passed its requirements, while values >1 meant a failure. So matrix positions with colors of blue to green represented passing design combinations, while those with colors of yellow to red represented failed combinations.

In the first design space plot (LE-LE vs wire length) which was applicable only to the 1st of 10 designs shown in Figure 3, the results with 26 nm MRC showed normalized DOF values for design elements with LE-LE of 41 nm and above achieved specifications of 100nm or higher (Figure 7). The normalized MEEF plot showed that designs with LE-LE of 68 nm and above would achieve specifications of either 3.5 MEEF for smooth or 7 MEEF for line ends, while below 68 nm LE-LE, only LE-LE with 59 nm and wire length of 216 nm to 228 nm would achieve the same MEEF specification. By looking at these two individual plots for normalized MEEF and DOF, one could discern the limiting lithographic metric and design rule, which in this case was MEEF at LE-LE. However, there's another convenient way to plot the data to determine if a design combination passed BOTH MEEF and DOF, and that was a normailzed P/F plot as described on the right side in Figure 7.

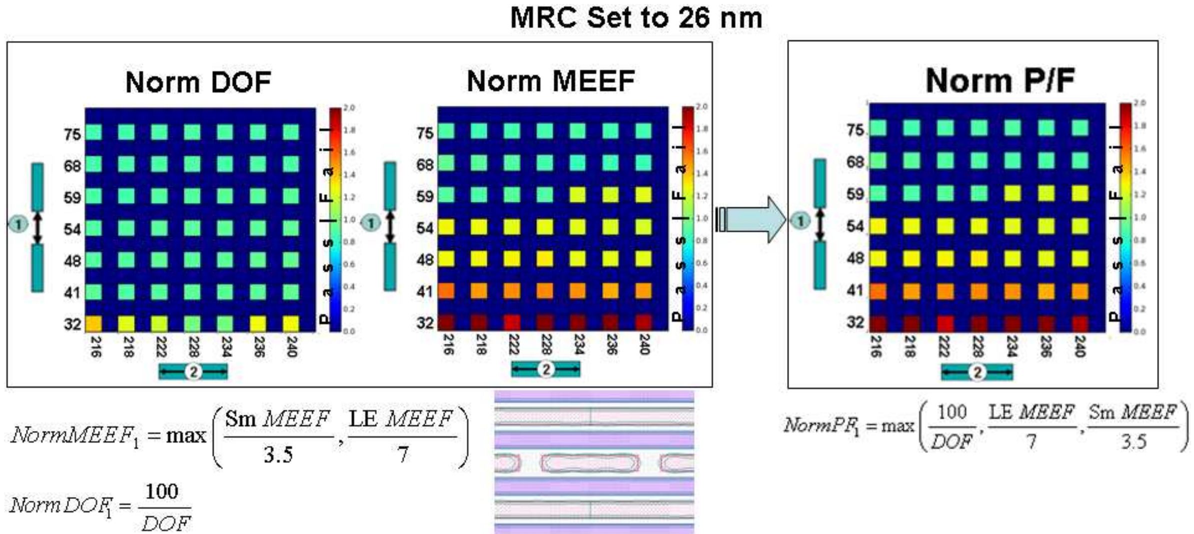


Figure 7. For design 1, normalized DOF and MEEF showed that LE-LE spacing is the limiting rule and that limitation was MEEF dominated. Normalized P/F plot was a combine plot for both metric.

In the second design space plots (LE-route space vs route width) which was applicable for the 2nd to 10th designs as shown in Figure 3, the results with 26 nm MRC showed normalized DOF values for design elements with LE route space of 48 nm and above with any route width above 65 nm generally achieved specifications of 100nm or higher (Figure 8). As in the plots for design 1, this DOF result of not being a lithographic limitation also seemed to hold true throughout the various routing designs 2-8. The normalized MEEF plots showed that only designs 2 and 3 have MEEF failures with respect to route width variations. By focusing just on the normalized MEEF plots for design 2 and 3, almost all designs with route width at 77 nm or lower had MEEF failures, while LE route spacing from 48 nm and above had no MEEF issues. Since BEOL routing layers were generally auto routed, the routing routine did not care about the different routing design types, so lithographic failures of any combinations of routing design rules was more critical than consideration of design types. So again in addition to the convenience of a single pass/fail plot, it was necessary to analyze this data with respect to one normalized P/F plot as shown in Figure 9, so that the route rules analysis was limited to the worse performance combinations of all relevant design types.

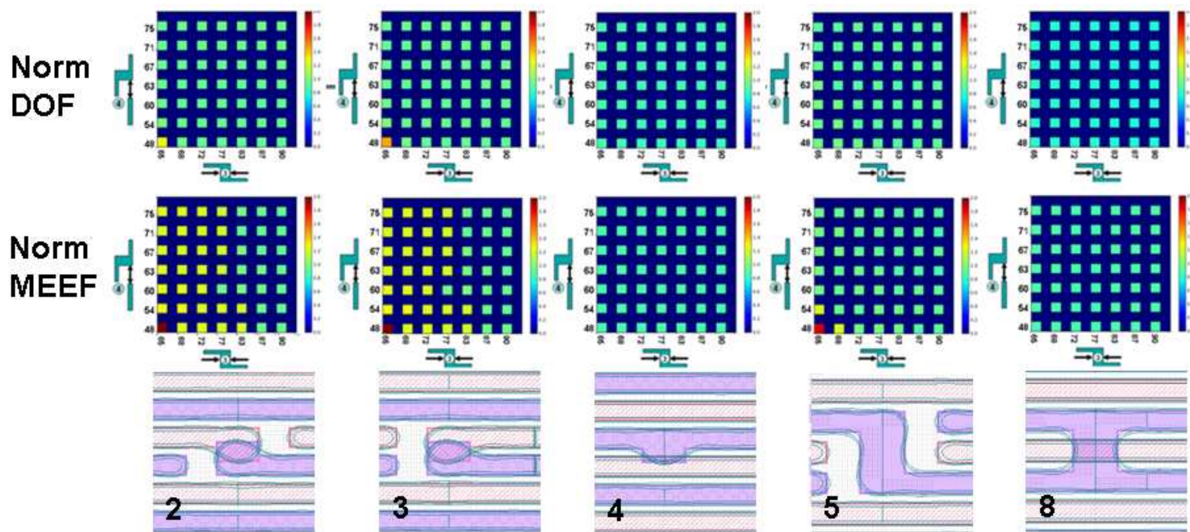
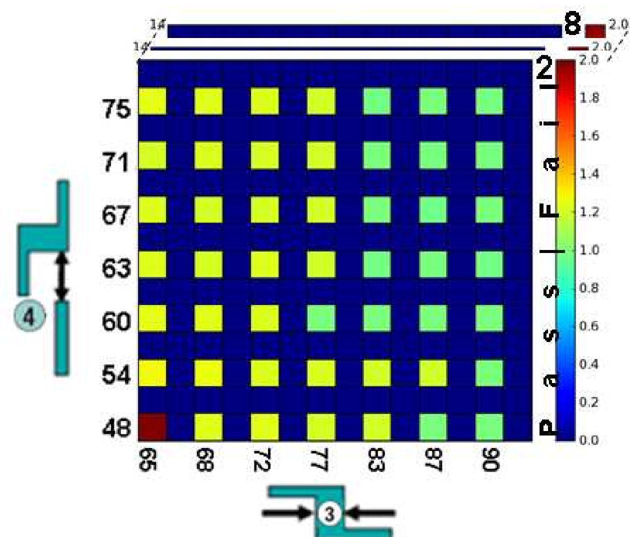


Figure 8. Normalized DOF and MEEF plots across designs with LE-route space and route width rules for designs 2-5 and 8. Designs 5a,6,6a, and 7 had similar results to 5 and 8. Designs 2 and 3 had the most limitations due to MEEF impact across different route widths. DOF did not appear to be limiting the design spaces and any of these designs.



$$NormPF_{2-8} = \max_{designs_2-8}\left(\frac{100}{DOF}, \frac{\mathrm{LE}\,MEEF}{7}, \frac{\mathrm{Sm}\,MEEF}{3.5}\right)$$

Figure 9. Normalized pass/fail metric for LE-route space and route width rules is a convenient singular plot that combines the normalized DOF and MEEF metric across all design types with these rules.

By analyzing the plots in Figures 7 – 10, two primary trends needed to be further investigated. The first trend of LE-LE distance vs MEEF showed that LE-LE distances at or below 54 nm had MEEF failures (Figure 7). Figure 10 displayed the MEEF maps for some specific LE-LE design rules around 54 nm. These maps contained in color pixel information along image edges that indicate the level of MEEF being experienced at each pixel location. In Figure 10a, a MEEF map of a 59 nm LE-LE with 216 nm wire length showed that the MEEF at the line end edges was yellow representing a MEEF somewhere between 5 and 6 (passes spec of 7). The corresponding mask for this design had the mask edges

separated by 27 nm, which was close to the MRC limit of 26 nm. As the LE-LE design shrinks to 54 nm (Figure 10b), the mask separation must also be reduced to achieve convergence in cost function to bring nominal image on target, but due to MRC, the mask separation could not be reduced any further than 26 nm. The MEEF map for 54 nm LE-LE design in Figure 10b showed that line end convergence along with MRC compliance can be achieved by merging of 2 main mask features, but this did not resolve the MEEF failure observed. The MEEF issue arose due to a relatively big mask polygon connection at the line end, whereby any mask sizing variation in this low contrast region would induce a large imaging shift (high MEEF). By reducing MRC and segmentation size limits, MEEF issue at LE-LE was improved as shown in Figure 10c. Just to also clarify the coloring in the MEEF maps for Figure 10, the MEEF map coloring for line ends in Figure 10b (MRC 26 nm) was red representing > 7 MEEF, while the coloring for line ends in Figure 10c (MRC 20 nm) was orange representing 6 > MEEF > 7. The mask limit reduction allowed the mask edges to approach closer to each other without introducing a large enough of a polygon shape that would be susceptible to large imaging shift when mask sizing variation was introduced. Lithographically valid LE-LE design rules down to 41 nm was possible at the reduced MRC constraint of 20 nm (Figure 12).

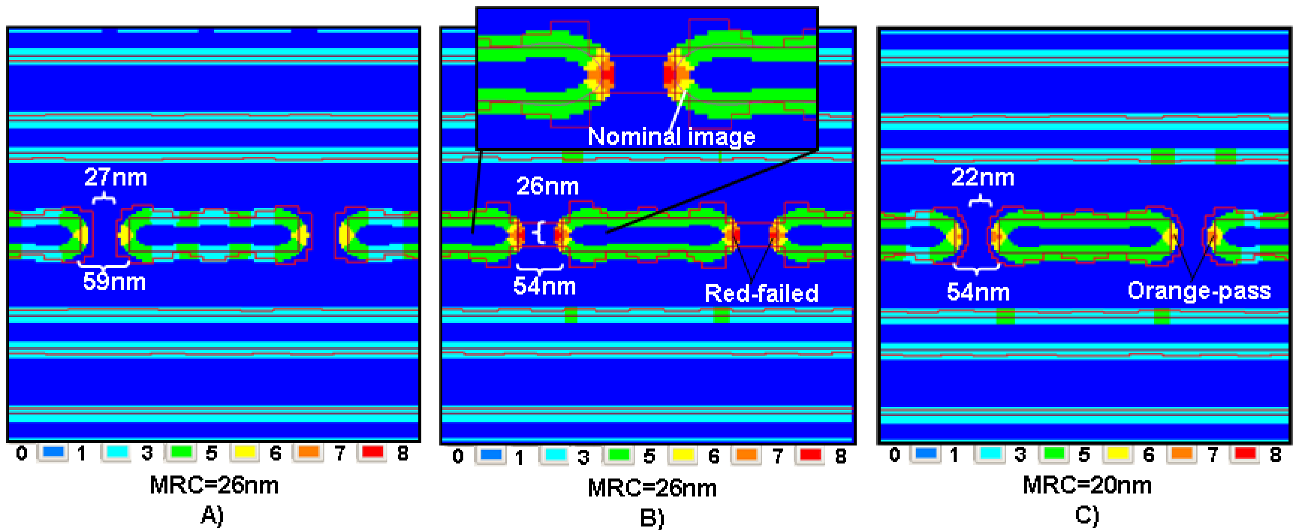


Figure 10. Reduction in MRC and mask segmentation size did improve MEEF on LE-LE.

The second observed trend was that MEEF failure occured as route width was decreased below 83 nm. Figure 11a and 11b showed the MEEF maps for route widths of 77 nm and 72 nm with LE route spacing of 60 nm, and in this situation the MEEF problematic region occured on the orthogonal facing edge of the route width. This smooth region's MEEF was yellow signifying a MEEF between 5 and 6, which was greater than the 3.5 MEEF specification. As the route width design reaches 72 nm, the mask edge parallel to the neighboring line edge had to grow closer to the neighboring edge so as to bring image convergence on the route width edge. As that mask edge approached the neighboring edge, the MEEF on the smooth region of the neighboring edge failed for MEEF. The MEEF on the line end was also yellow, but this was passing as the MEEF requirement on line end was 7. Similar to the first observed trend, MEEF on the smooth edge could be improved with reduction of mask MRC and segmentation. As shown in Figure 11c, at MRC of 20 nm, the route width mask edge was allowed to be within 25 nm of the neighboring smooth edge with finer segmentation. This allowed for the convergence of the route width edge without introducing larger segmented mask polygon, which would be more susceptible to inducing larger image shift with mask sizing variation.

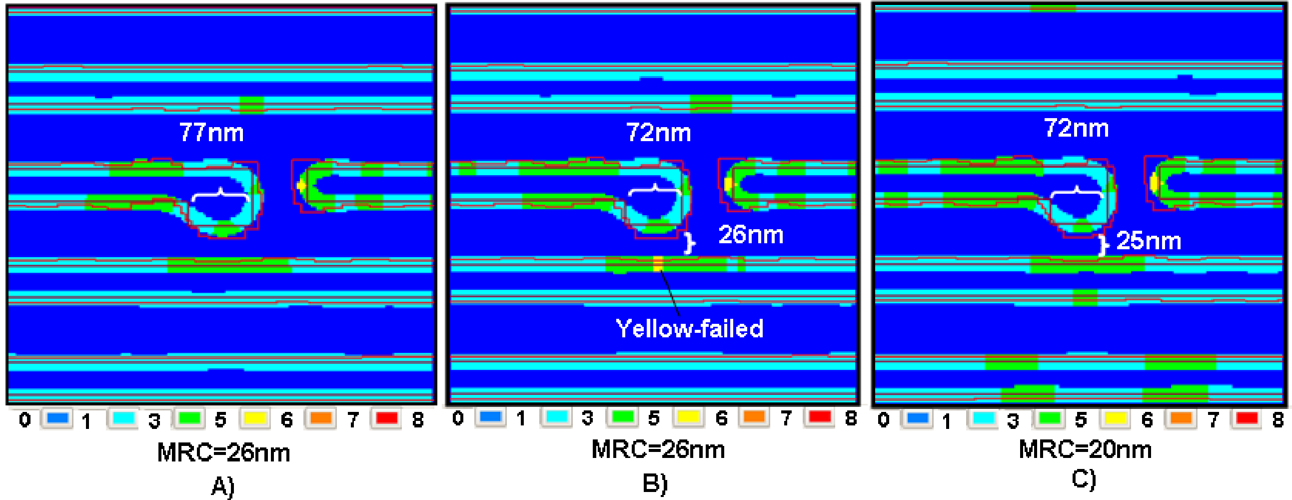


Figure 11. Reduction in MRC and mask segmentation size can improve MEEF performance as route widths shrinks.

The realized improvements in MEEF performance on these singular test cases were expanded to the entire design space for analysis with variation in MRC. The normalized P/F metric which contained both DOF and MEEF lithographic criteria results in Figure 12 showed the reduction in MRC from 26 nm to 20 nm led to ~70% of the design space passing from ~37%. As MRC was further reduced to 14 nm, there was not any significant improvements to the P/F metric. The trends within each of these plots remained relatively similar in that LE-LE and route width performances dictated design space passing rate.

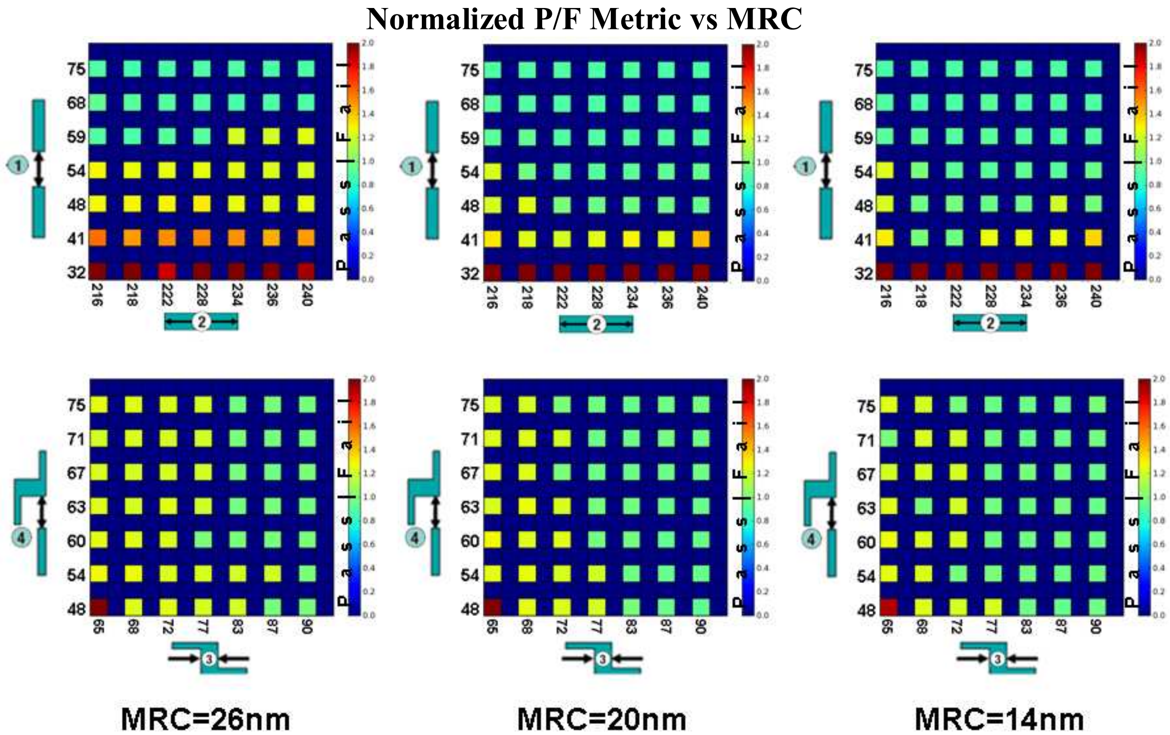


Figure 12. Normalized P/F metric indicated significant improvements could be made to design rule space fulfillment by the reduction of MRC from 26 nm to 20 nm, but no more significant improvements was reaped by further reduction of MRC to 14 nm.

4. CONCLUSIONS

Using DRD-SMO flow, it was determined that mask MRC reduction contributed to improvements in design rule space for 60 nm pitch BEOL routing designs. In particular problematic MEEF at LE-LE spacing and route widths were alleviated by reducing MRC from 26 nm to 20 nm, but reduction to 14 nm did not yield any further improvements to the design space. DOF was generally not an issue for any of the designs as the decomposed single layer pitch was at 120 nm in double patterning. At 20 nm MRC, a 70% passing rate of this set of design rule space was achieved.

ACKNOWLEDGEMENTS

The authors of this paper would like to acknowledge members of TI's OPC/Lithography team members Jim Blatchford, Steve Prins, Scott Jessen, and Ryoung-han Kim for their design set, valuable inputs, feedback and guidance.

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