

# Evaluation of Inverse Lithography Technology for 55nm-node memory device

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## ABSTRACT

Model based OPC has been generally used to correct proximity effects down to ~50 nm critical dimensions at  $k_1$  values around 0.3. As design rules shrink and  $k_1$  drops below 0.3, however; it is very hard to obtain enough process window and acceptable MEEF (Mask Error Enhancement Factor) with conventional model based OPC. Recently, ILT (Inverse Lithography Technology) has been introduced and has demonstrated wider process windows than conventional OPC. The ILT developed by Luminescent uses level-set methods to find the optimal photo mask layout, which maximizes the process window subject to mask manufacturing constraints.

We have evaluated performance of ILT for critical dimensions of 55nm, printed under conditions corresponding to  $k_1 \sim 0.28$ . Results indicated a larger process window and better pattern fidelity than obtained with other methods. In this paper, we present the optimization procedures, model calibration and evaluation results for 55 nm metal and contact layers and discuss the possibilities and the limitations of this new technology.

**Key words:** Inverse Lithography Technology, Process window, Model calibration, OPC, RET, MEEF

## 1. Introduction

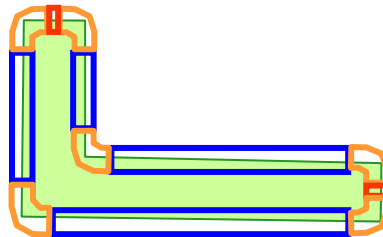
As semiconductor manufacturers move to advanced nodes of 65nm, 45nm, 32 nm, and below, lithography becomes more challenging because it is fundamentally constrained by basic principles of optical physics. At 65 nm node, a line width is less than a third of the exposing wavelength. Exposure systems for 45nm and 32 nm processes will use the same wavelength, and will benefit from only modest improvements in numerical aperture. This has prompted increased effort into finding photo mask patterns and illuminator configurations to print the smaller patterns with maximum process windows. The inverse lithography problem resembles the corresponding optical problem of retrieving an object from its image. Approaching the inverse lithography problem in this manner dates back to the 1980s, starting with the pioneering work of B. E. A. Saleh and his students<sup>[1,2]</sup>. The inverse lithography problem differs from the object retrieval problem in one important respect; because the image is formed in photo resist with very high contrast, only those parts of the intensity function near resist edges determine their positions. Another way of looking at this is that much of the information in the intensity function is lost in the process of forming resist patterns. We can use this to advantage to do more than optimize pattern accuracy under nominal exposure and process conditions. Inverse lithography solutions can maximize contrast or depth of focus, or minimize MEEF in addition to controlling nominal dimensions of patterns. If we define an objective cost function as the sum of terms characterizing edge placement errors under multiple exposure, defocus, and MEEF conditions, we can describe the ILT solution as a search for its minimum over the vector space that describes possible mask patterns.

Earlier approaches to ILT often produced photo mask solutions with superior image performance, but it was impractical to manufacture them with available methods, and computation requirements were excessive for large designs. In order to deal with these issues, we must impose constraints on the search for the minimum value of the cost function, and employ efficient algorithms on a distributed computing platform. A suitable set of algorithms is based on

level-set methods, originally developed to solve problems of boundary motion governed by differential equations, and later applied to searches for extreme<sup>[3]</sup>. The level-set representation allows mask patterns to take more general shapes than can be easily expressed as polygons created by perturbations of segmented targets, the most common representation used in model based OPC. It also allows formation of sub-resolution assist features (SRAFs) during inversion to further minimize the cost function. In order to enforce mask manufacturing rules (MRC) the ILT solution becomes a constrained optimization. Taking account of the need to comply with MRC throughout the search process minimizes the adverse consequences of mask rules on the process window obtained with the inverse solution.

### 1.1. ILT Method

Because inverse lithography is a problem of optimization, it is necessary to define a target pattern and a measure of how far the solution deviates from the target, which appears in the cost function to be minimized. Both of these definitions deserve careful consideration. An unmodified circuit layout is often not the best choice for the target. For convenience, layouts usually consist of polygons with right angles, but minimizing the radius of curvature at corners is often less important than getting dimensions right elsewhere. Due to the band-limited nature of optical imaging, trying to force the solution to converge to small radii at corners can waste computing cycles with no improvement in quality. One method to address this is to round corners of pattern layouts to create more suitable targets. Another is to divide target patterns into line ends, corners, jogs, and long straight edges so that we can apply different weights and tolerances to image deviations in each type of region. Figure 1 shows an example of a target pattern divided into such regions. Once the target pattern is defined, it is necessary to select a measure by which computed resist contours deviate from it, such as the sum of square distances integrated along each contour. The method employed in this work is to divide the image space into pixels, and for each pixel containing an image contour, measure the mean distance between the contour and the nearest point of the target. Because SRAFs are created as part of the ILT solution, it is essential to examine all pixels to ensure that side lobes do not print at large distances from target pattern. These distance measurements form the basis for a cost function, which the inverse lithography solution will minimize by finding an appropriate mask pattern.



**Figure 1.** Classification of corners, line ends, and long straight edges to apply different weights and tolerances in the cost function for a target polygon.

Capturing the full benefit of inverse lithography requires that the cost function include terms describing multiple images. If it is desired to improve contrast, depth of focus, or sensitivity to mask pattern errors, it is necessary to minimize the cost function and its derivatives with respect to an appropriate set of variables. The following is the general form of a cost function that includes multiple images and edge types as classified in Figure 1.

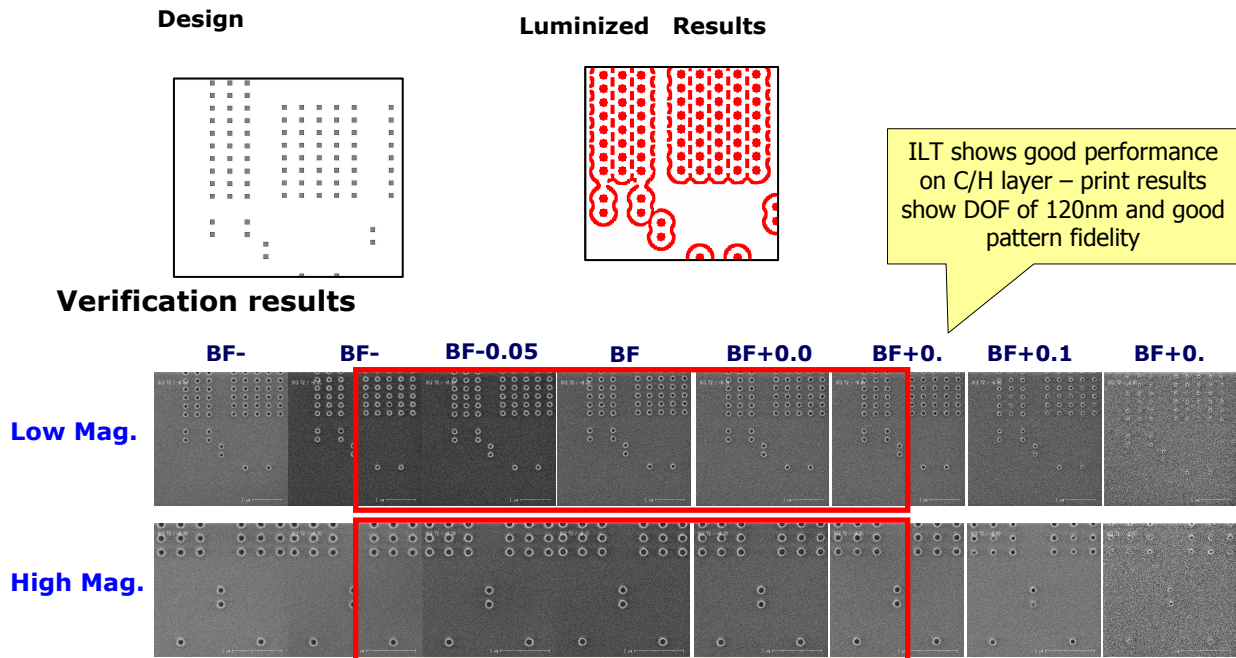
$$H = \sum_{\text{pixels}} \sum_{\text{Exp,Def}} w_{(\text{Exp,Def})} \sum_{\text{edgetype}} w_{\text{edgetype}} |f(\Psi) - \Phi|$$

Here  $f(\Psi)$  is the image of the mask function  $\Psi$ ,  $\Phi$  is the target pattern, and the sets  $w$  are weights assigned to image deviations for different edge types and exposure conditions. We compute functional gradient of the cost function with respect to the mask pattern,  $\nabla_{\Psi} H$ , in order to find the ILT solution<sup>[4,5]</sup>. Mask constraints appear as forbidden regions in the vector space on which  $\Psi$  is defined. Choices of exposure conditions and their weights that appear in  $H$  determine the sizing and placement of both main features and SRAFs in the ILT solution. By appropriate selection of the off-focus terms and their weights, the ILT solution can either minimize deviations of nominal patterns, or encapsulate functions otherwise performed by DFM re-targeting to improve depth of focus.

## 2. Results and Discussions

### 2.1. Random contact windows implementation

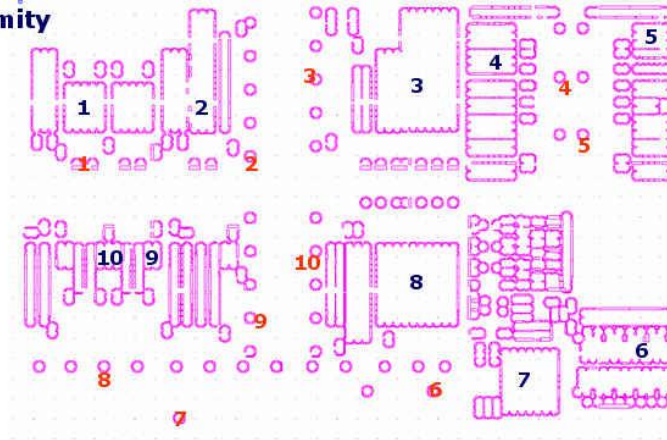
Figure 2 shows mask design, luminized layout (the layout for correction) and wafer print results for random contact windows. This study demonstrated the random contact windows pattern fidelity with wider process margin and good CDU (Critical Dimension Uniformity) on wafer. KrF Scanner ( $\lambda=248\text{nm}$ ), exposure (NA= 0.8) with annular type illumination condition were used. An attenuated phase-shifting mask (6% Att. PSM) with Manhattan constraints was used to simulate with Luminescent ILT. The process window obtained useful DOF of 120 nm at 10% exposure latitude with good pattern fidelity.



**Fig. 2:** Target and luminized layout. Verification results for random contact windows by using KrF scanner.

Figure 3 shows ID (Isolated-Dense) bias  $\sim 12\text{nm}$ . It is better performance than Hynix's conventional manual OPC method but worse than ArF process without tuning the mask bias. This bias can be fixed by using the mask bias.

# CD uniformity



	MP1	MP2	MP3	MP4	MP5	MP6	MP7	MP8	MP9	MP10	AVE.
Dense C/H D1CD	102.1	112.4	106.7	112.0	109.8	105.8	114.3	117.3	112.3	114.8	110.8
Iso. C/H D1CD	100.0	99.0	106.2	91.0	100.6	90.5	101.3	97.3	104.3	95.5	98.6

Fig. 3: ID (Isolated-Dense) bias ~ 12nm at KrF random contact hole without the calibration.

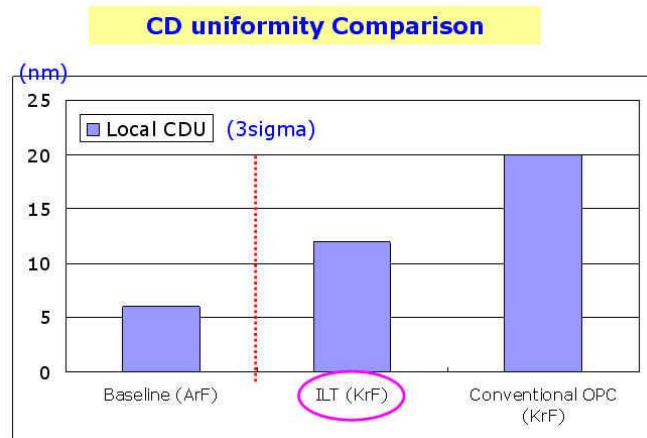


Fig. 4: CD Uniformity comparison of random contact windows with ArF and KrF (Conventional OPC vs. ILT OPC)

The initial wafer results demonstrated ILT with KrF scanner potentially can replace baseline process with ArF scanner. The LCDU (12nm) with ILT OPC improved 40% compared to conventional model based OPC simulation tool (20nm). Further optimization, including model calibration, will improve LCDU. If successful, this replacement can bring great benefits; reduced CoO due to extending the KrF scanner life, reduced cost in materials such as resist, BARC and mask blanks in existing manufacturing line.

2.2. Pattern fidelity improvement

Figure 5 compared process margin with baseline with ILT results. The process margin does not improve because not enough space to insert assist features results no significant margin improvement. But the pattern fidelity improved on these complex patterns (see Fig. 6).

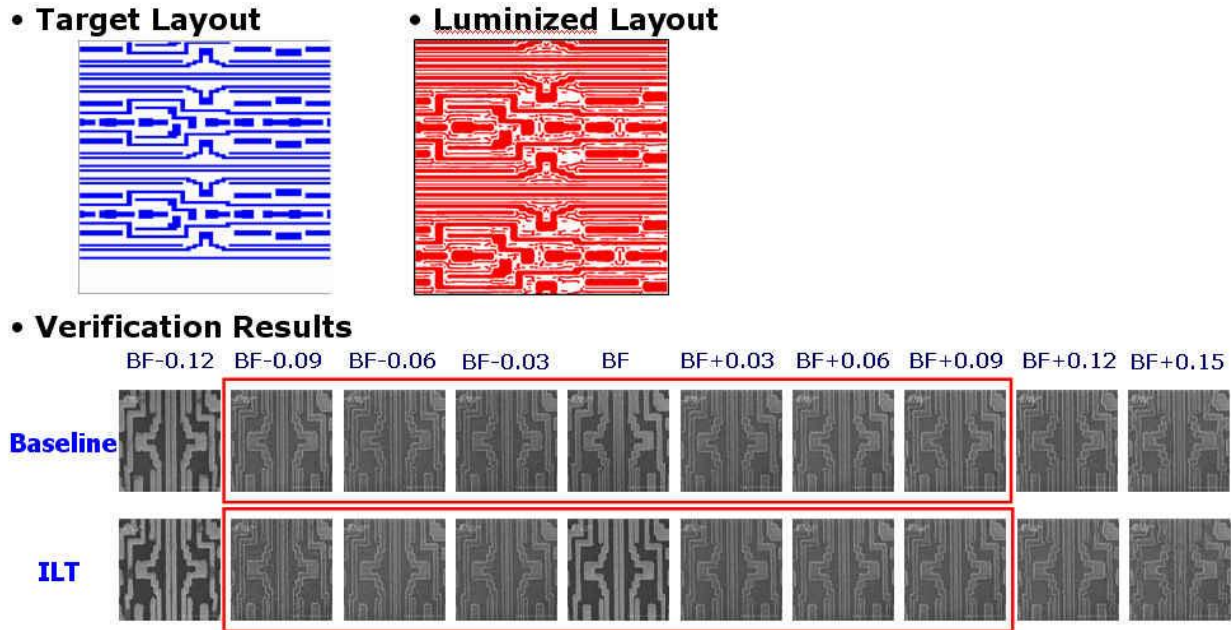


Fig. 5: Target and luminized layout, Verification Results with ArF complex line and space

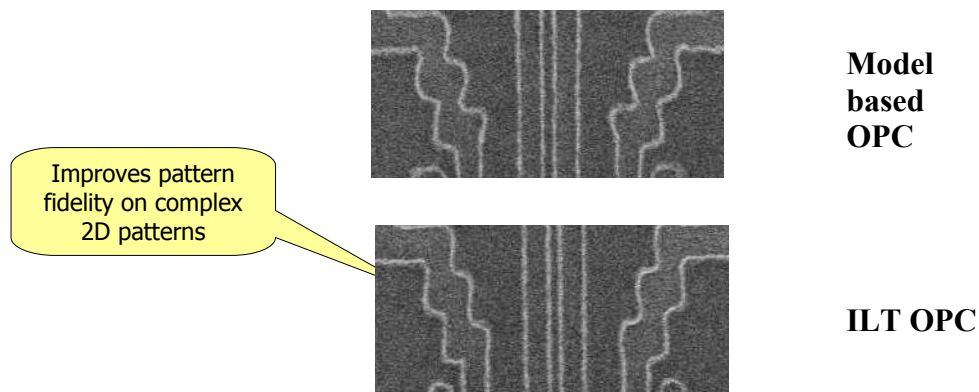


Fig. 6: Comparison pattern fidelity between Model base OPC and ILT OPC

### 2.3 Low-k1 memory device application and Cell optimization

In previous ILT implementations, the mask rule constraints were not considered, resulting in masks with curved geometry and many small fragments. Such mask are challenging for mask manufacturing including in e-beam writing, inspection, and repairs. In Luminescent's ILT approach, MRC are built into the inversion solver. We specify the various MRC including SRAF and 30nm on the Manhattan shaped mask.

Fig. 7 shows design target and ILT simulated layout in various one/two band AF and no MRC/MRC conditions. The memory devices leads the low k1 RET by using manual cell optimization which is the most critical area to drive the technology. ILT approach can save the evaluation time and increase the accuracy for cell optimization. Figure 7 demonstrated the solution for low-k1( $\sim 0.28$ ) cell optimization at layer boundary. According to the simulated results, two-band AF w/ MRC(30nm) is the best solution considering manufacturability by using ArF immersion lithography.

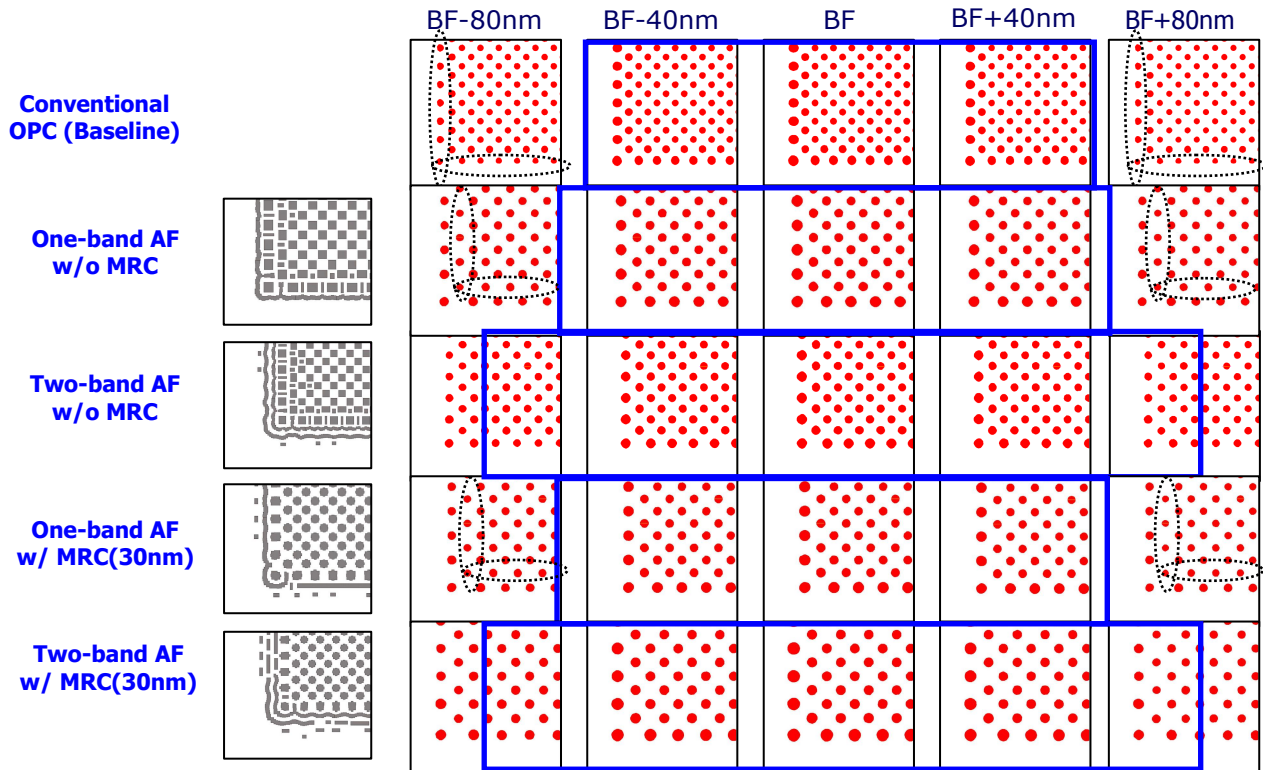


Fig. 7: Design and simulated ILT layout in various one/two band AF, no MRC/MRC condition with process windows

#### 2.4. MRC requirements vs. process windows

In order to maximize the process windows with present enabling mask capability especially minimum feature size resolution, we make a split test for no SRAF/ with SRAF and MRC 20nm/25nm/30nm. As shown Figure 8, the best process windows can be achieved with SRAF/ MRC 25nm below conditions in boundary area. During the inversion calculation, mask rule constraints, especially minimum feature size and area are checked. The resulting Manhattan shaped mask is constrained to satisfy the specified mask rules. The production worthy mask demonstrated the larger process windows (100nm) at the corner compared to no SRAF mask (40nm). This ILT corrected mask provides substantially improved process windows with the optimal manufacturable mask design. We obtained larger DOF for features at edges of dense arrays and in peripheral areas. In further improvement for the depth of focus and exposure latitude, the mask capability can help to enable to improve the process windows with the present scanner without the further investment such as the extreme higher immersion NA scanner and EUV lithography with ILT solution.

#### 2.5. Future Work

The experiment results show ILT is very efficient on random contact layer in terms of the wider process window and good pattern fidelity. We will expand this to full-chip level. Full chip global CDU will be evaluated, and mask manufacturability will also be evaluated on mask lever for rule/model-based MRC. In addition to full-chip level, further cell optimization using ILT compared to OPC will be studied along with source optimization consideration.

### 3. Conclusion

We have applied inverse lithography to memory contact and line-space layers with critical dimensions of 55 nm, corresponding to  $k_1 \sim 0.28$ . The main benefits we obtained were following: 1). With ILT and its built-in model based SRAF, we potentially can move certain layers from ArF scanner to KrF scanner; 2). ILT improves the pattern fidelity on complex 2D structures where it is difficult for OPC to correct; 3). For memory cell contact array larger

process windows are obtained for features at edges of dense arrays and in peripheral areas. In the interior of dense arrays, where space is not available to insert SRAFs, CD uniformity and depth of focus with ILT are similar to that obtained with other methods. Because illuminator design is optimized for the dense arrays, their peripheries and isolated patterns generally exhibit lower depth of focus, so the net effect is a larger common process window with ILT. MRC constraints in some cases affect the magnitude of improvement we obtain with ILT. Improvements to mask manufacturing technology, particularly inspection, will permit us to get increased benefits from ILT as CDs shrink below 55 nm.

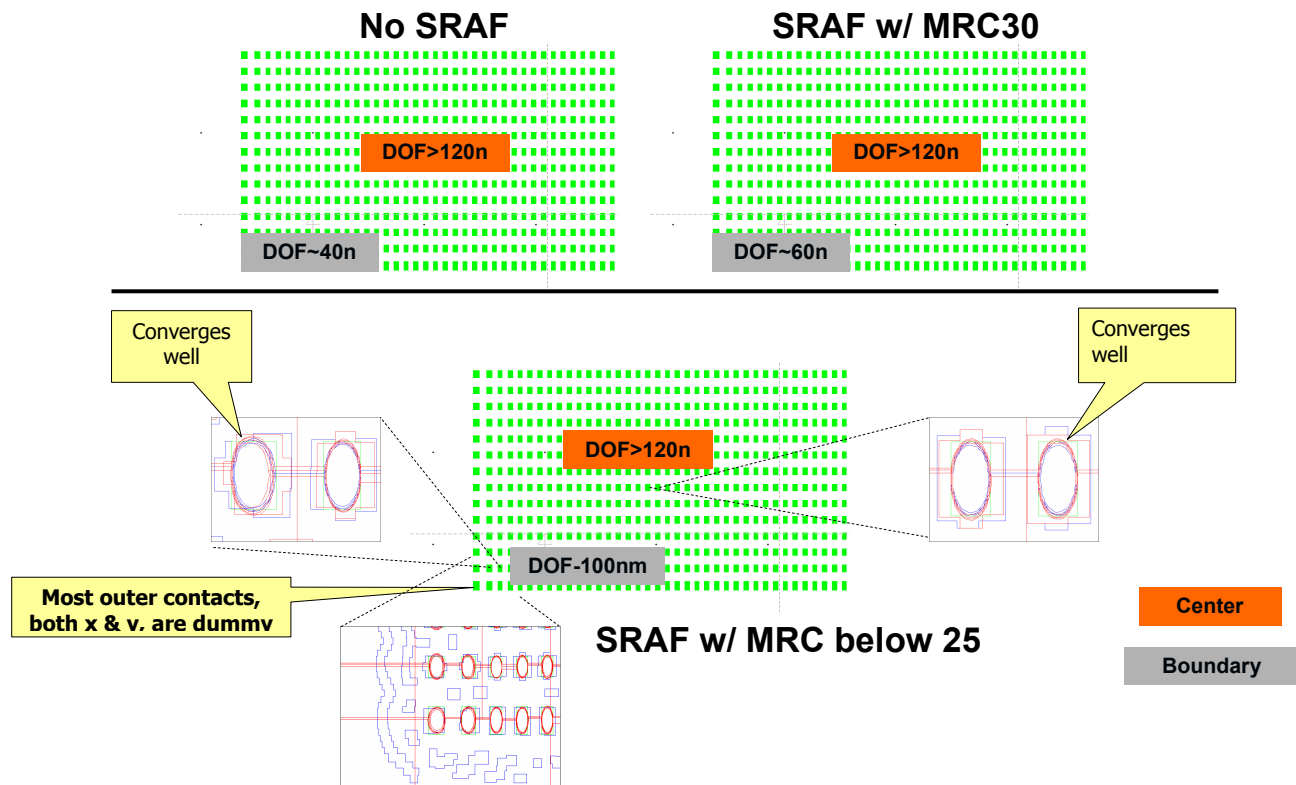


Fig. 8: Mask requirements for process windows improvement with SRAF with various MRC

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