

Exploration of Complex Metal 2D Design Rules Using Inverse Lithography

Simon Chang^{a*}, James Blatchford^a, Steve Prins^a, Scott Jessen^a, Thuc Dam^b, Guangming Xiao^b,
Linyong Pang^b, Bob Gleason^b

^a Texas Instruments, Inc., Dallas, TX
^b Luminescent Technologies, Inc., Palo Alto, CA

ABSTRACT

As design rule (DR) scaling continues to push lithographic imaging to higher numerical aperture (NA) and smaller k_1 factor, extensive use of resolution enhancement techniques becomes a general practice. Use of these techniques not only adds considerable complexity to the design rules themselves, but also can lead to undesired and/or unanticipated problematic imaging effects known as “hotspots.” This is particularly common for metal layers in interconnect patterning due to the many complex random and bidirectional (2D) patterns present in typical layout. In such situations, the validation of DR becomes challenging, and the ability to analyze large numbers of 2D layouts is paramount in generating a DR set that encodes all lithographic constraints to avoid hotspot formation.

Process window (PW) and mask error enhancement factor (MEEF) are the two most important lithographic constraints in defining design rules. Traditionally, characterization of PW and MEEF by simulation has been carried out using discrete cut planes. For a complex 2D pattern or a large 2D layout, this approach is intractable, as the most likely location of the PW or MEEF hotspots often cannot be predicted empirically, and the use of large numbers of cut planes to ensure all hotspots are detected leads to excessive simulation time. In this paper, we present a novel approach to analyzing full-field PW and MEEF using the inverse lithography technology (ILT) technique, [1] in the context of restrictive design rule development for the 32nm node. Using this technique, PW and MEEF are evaluated on every pixel within a design, thereby addressing the limitations of cut-plane approach while providing a complete view of lithographic performance. In addition, we have developed an analysis technique using color bitmaps that greatly facilitates visualization of PW and MEEF hotspots anywhere in the design and at an arbitrary level of resolution.

We have employed the ILT technique to explore metal patterning options and their impact on 2D design rules. We show the utility of this technique to quickly screen specific rule and process choices—including illumination condition and process bias—using large numbers of parameterized structures. We further demonstrate how this technique can be used to ascertain the full 2D impact of these choices using carefully constructed regression suites based on standard random logic cells. The results of this study demonstrate how this simulation approach can greatly improve the accuracy and quality of 2D rules, while simultaneously accelerating learning cycles in the design phase.

Keywords: Design rule, OPC, lithography simulation, metal patterning

*s-chang8@ti.com

1. INTRODUCTION

Over the last few process technology nodes, due to smaller k1 factor and subsequent extensive use of resolution enhancement techniques (RET), design rule (DR) complexity has increased enormously. To counter the ever-increasing design rule complexity, restricted structure approaches, such as single-orientation and gridded layout, had been successfully implemented on some front-end-of-line (FEOL) patterning layers. For interconnect patterning layers in the back-end-of-line (BEOL), especially the first metal layer, such restricted structure approaches are difficult to implement due to the many complex random and bidirectional (2D) patterns present in typical layout. In such situations, the validation of metal design rules becomes challenging, and the ability to analyze large numbers of 2D layouts is paramount in generating a design rule set that encodes all lithographic constraints to avoid hotspot formation.

Process window (PW) and mask error enhancement factor (MEEF) are the two most important lithographic constraints in defining design rules. Getting a good handle on these two constraints is essential to a robust design rule set. In this paper, we present a novel approach to analyzing full-field PW and MEEF using the inverse lithography technology (ILT) technique, [1] in the context of restrictive design rule development for the 32nm node. We also present simulation flows to explore metal patterning options and their impact on 2D design rules using the ILT. We further demonstrate how these techniques can be used to ascertain the full 2D impact of these choices using carefully constructed regression suites based on standard random logic cells. The results of this study demonstrate how this simulation approach can greatly improve the accuracy and quality of 2D rules, while simultaneously accelerating learning cycles in the design phase.

2. METHODOLOGY AND SIMULATION RESULTS

2.1 Inverse Lithography Technology (ILT)

Inverse Lithography techniques have been used here to address several simulation limitations faced in interconnect patterning. One of the key limitations is the metrology flexibility. Traditionally, characterization of PW and MEEF by simulation has been carried out using discrete cut planes. For a large 2D layout or a complex 2D pattern as illustrated in Figure 1a, this approach is intractable, as the most likely location of the PW or MEEF hotspots often cannot be predicted empirically, and the use of large numbers of cut planes to ensure all hotspots are detected leads to excessive simulation time.

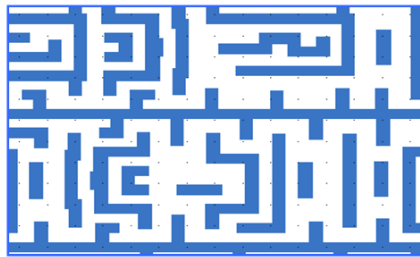


Figure 1a. A typical 2D metal layout (drawn).

Our ILT approach uses metrology “topologies” [1] to cover all pattern feature types as illustrated in Figure 1b. Although the “topologies” are by default placed automatically, additional topologies can be placed manually anywhere in the design to allow lithography analysis by regions or spots. Additionally, each topology can be weighted differently in the inversion’s Cost Function (E) calculation so that mask pattern correction and source mask optimization are weighted toward the care-about parts of the pattern, such as line ends, smooth edges, etc.

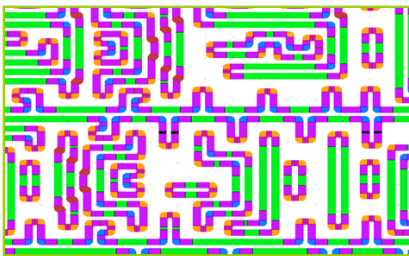


Figure 1b. A 2D metal layout with topologies.

Figure 1c shows the same 2D metal layout with pixel-based depth-of-focus (DOF) bitmaps after inversion and process window calculation. Two random hotspots were clearly visible, and the cause of these hotspots was later traced back to an over-sizing of a rectangular metal pad during the re-targeting step prior to inversion. Since this problem did not exist on the original drawn where metrology planes were initially defined, these random hotspots could not be predicted and therefore caught by discrete cut planes.



Figure 1c. A 2D metal layout with pixel-based color bitmaps that show random hotspots.

2.2 Design Rule Exploration using Parameterized Structures

In this section, parameterized structures such as those illustrated in Figure 2 are used for 2D simulation to explore metal line-end design rules. This structured module consists of hundreds of sub-cells in which each sub-cell has a metal line-end structure with three design variables. These three design variables are space between two line-ends (G), metal width (W), and space between metals (S). Each variable varies over a range of design space, and each sub-cell has unique variable $\{G, W, S\}$ set. The entire structured module was then inverted in parallel through distributed computing. Depth-of-focus (DOF) and Mask Error Enhancement Factor (MEEF) from each sub-cell were then analyzed and compared to pre-defined criteria. Figure 3 illustrates a design rule exploration flow for a single design rule using parameterized structures. By comparing the simulation results to pre-defined criteria, we can determine initial design rules for metal line-ends. If the initial design rules cannot support design requirements, we can repeat the same flow to explore different illumination conditions, different inversion approaches (to be discussed later in the paper), different sub-resolution assist features (SRAF), etc. The same flow can be expanded to support multiple design rules as well. For the case illustrated in Figure 2, the goal is to find metal width (W) and metal space (S) combinations that support a design rule of 50nm line-end space (G).

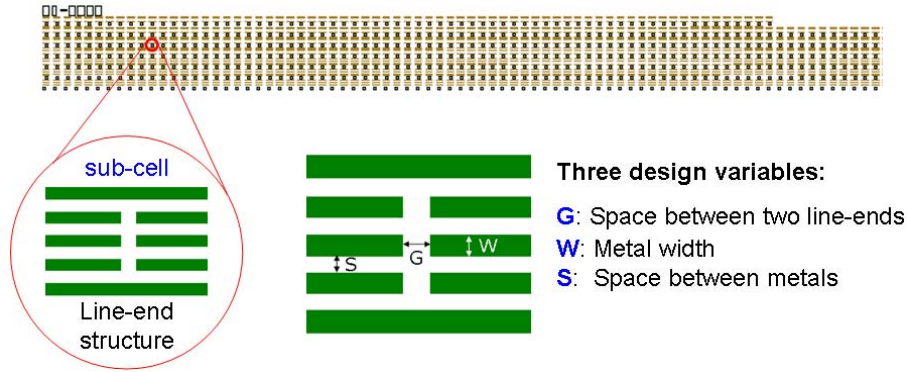


Figure 2. Parameterized structures used to explore metal line-end design rules.

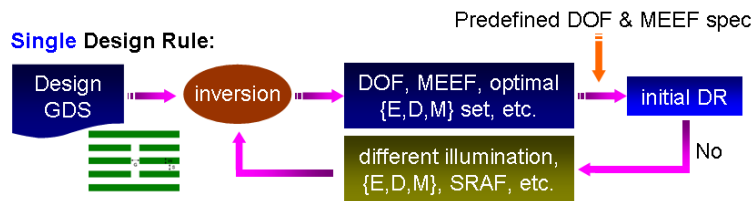


Figure 3. A design rule exploration flow using parameterized structures (single design rule).

Figure 4 shows MEEF results plotted against metal space and line-end space for different metal widths (W). Based on MEEF target of 5.0, the result in Figure 4 shows that 80nm is the minimum metal width that can support a 50nm line-end space at any metal space. The MEEF result can be re-plotted as shown in Figure 5(b) to emphasize MEEF variation as a function of metal width and metal space. Figure 5(b) shows the depth-of-focus (DOF) result plotted also as a function of metal width and metal space at 50nm line-end space. With a DOF target of $0.120\mu\text{m}$, the result confirms that 80nm metal width can support a 50nm line-end space in most cases. However, in some cases—the regions in pink color in Figure 5(b)—DOF drops below the target, an indication of litho margin issue. These cases involve width/space ratios that suggest either resist litho margin or trench litho margin has started to degrade. Proper re-sizing is one way to address these litho margin issues. In another word, DOF depends on width/space ratios. Based on MEEF and DOF results shown in Figure 5, it can be concluded that in order to support design rule of 50nm line-end space, metal width needs to be greater or equal to 80nm with proper re-sizing at certain width/space ratios.

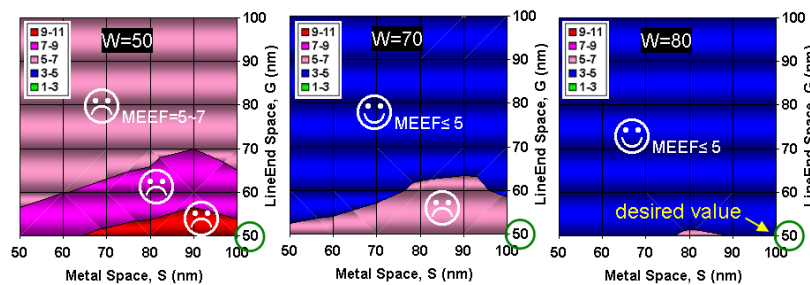


Figure 4. MEEF as a function of metal space and line-end space for various metal widths.

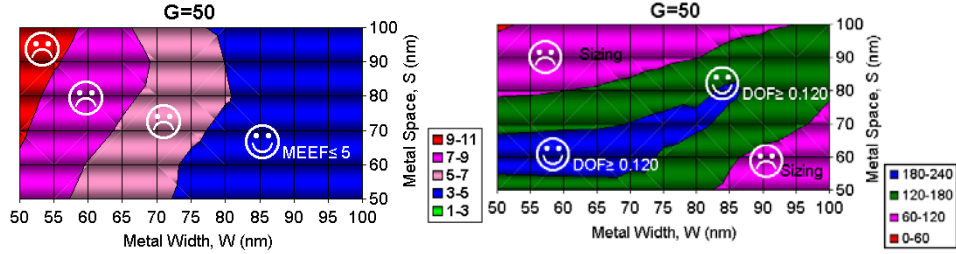


Figure 5. (a) MEEF as a function of metal width and metal space at 50nm line-end space. (b) DOF as a function of metal width and metal space at 50nm line-end space.

2.3 ED-aware Inversion vs. EDM-aware Inversion in the ILT

The conventional optical proximity correction (OPC) approach represents mask regions as segmented polygons. As such, the solutions are limited to perturbations of target patterns and are further restricted by segment placement. All degrees of freedom in OPC are significantly constrained to get CDs (critical dimensions) on target. In contrast, the ILT technique represents mask regions as continuous target patterns; therefore, its solutions are not constrained to resemble the target patterns. Without such a constraint, other degrees of freedom become available to optimize image contrast, DOF and MEEF in addition to getting CDs on target. In this paper, we discuss the importance of optimization on inversion variables and how adding mask bias to the inversion improves overall lithographic performance on complex 2D metal layouts.

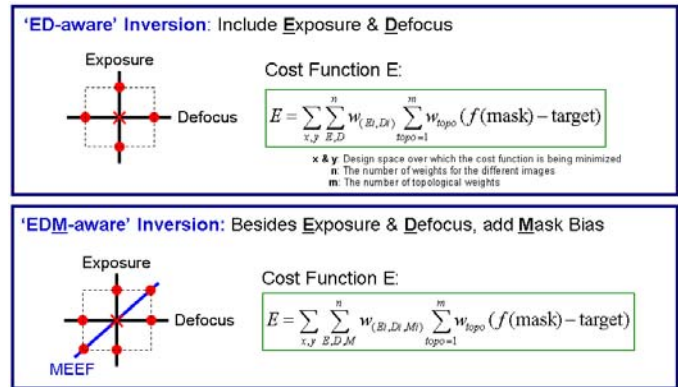


Figure 6. (a) ED-aware inversion and its Cost Function (b) EDM-aware inversion and its Cost Function.

Figure 6(a) shows “ED-aware” inversion schematically. Here, in the Cost Function equation, only exposure and defocus are included in mask pattern correction and source mask optimization. Figure 6(b) depicts “EDM-aware” inversion and its Cost Function equation where not only exposure and defocus but also mask bias are included in mask pattern correction and source mask optimization. As stated earlier, MEEF plays an important factor in low k1 lithography. Therefore, when exploring design rules for 32nm node, MEEF optimization is a necessary step. In this paper, we demonstrate that this step can be achieved by including mask bias in the inversion (EDM-aware inversion) while optimizing the weight of mask bias relative to the weight of exposure and defocus corrections. For comparison purposes, we also perform the corrections without including mask bias in the inversion (ED-aware inversion). The same line-end-parameterized structures were used here to illustrate how the step was carried out.

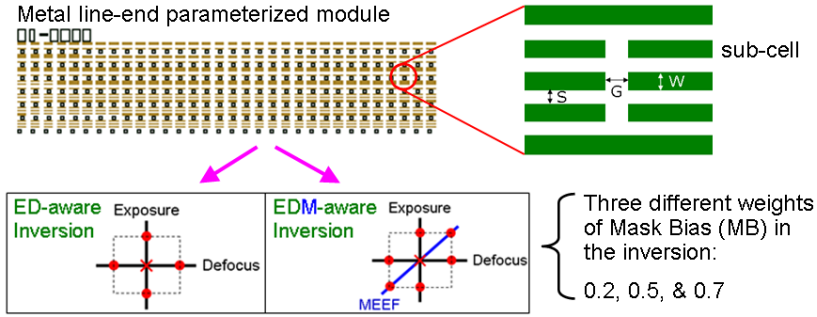


Figure 7. Basic setup of ED-aware vs. EDM-aware inversion using parameterized structures for metal line-end design rules.

Figure 7 illustrates the basic setup of ED-aware vs. EDM-aware inversion using parameterized structures for metal line-end design rules. This structured module was processed through ED-aware and EDM-aware inversions using distributed computing. During EDM-aware inversion, we also applied three different weights of mask bias to gauge how mask bias affects DOF and MEEF compared to an inversion without mask bias, i.e. ED-aware inversion. For each sub-cell, a MEEF delta was calculated by subtracting ED-aware MEEF from EDM-aware MEEF, and a DOF delta was calculated by subtracting ED-aware DOF from EDM-aware DOF. The MEEF delta is then plotted in x-axis and DOF delta in y-axis on a 2D-plot as shown in Figure 8.

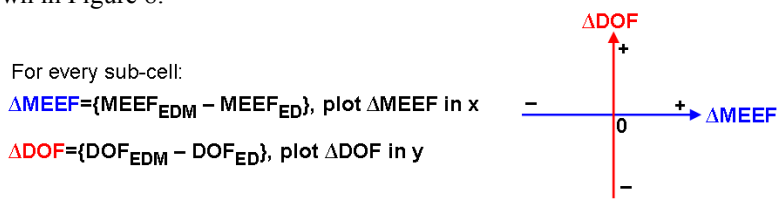


Figure 8. MEEF delta and DOF delta: EDM-aware inversion vs. ED-aware inversion.

Referring to the 2D $\Delta\text{MEEF}/\Delta\text{DOF}$ plot in Figure 8, data points in the $(-x, \pm y)$ quadrants indicates MEEF was improved over ED-aware inversion (MEEF number was reduced) and data points on $(+x, \pm y)$ quadrants indicates MEEF was degraded (MEEF number was increased). Data points on $(-x, +y)$ quadrant indicate both MEEF and DOF were improved. These plots are useful to visualize tradeoffs and differences between MEEF and DOF when different weighting factors for mask bias are during cost function optimization. Figure 9 shows DOF delta vs. MEEF delta with three different weights of mask bias.

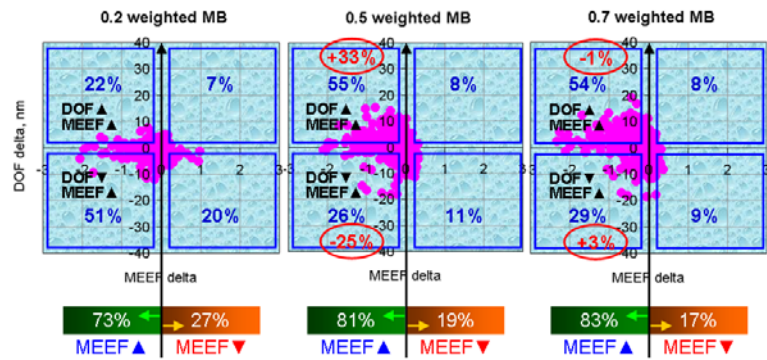


Figure 9. DOF and MEEF results with different weights of mask bias in inversion optimization. (a) 0.2 weighted mask bias (b) 0.5 weighted mask bias (c) 0.7 weighted mask bias.

The result in Figure 9(a) indicates 73% of sub-cells showed improved MEEF when some mask bias was added to the inversion optimization. Figure 9(b) shows the percentage was increased to 81% when the weight of mask bias was increased from 0.2 to 0.5. Note that the data spread in the y-axis (DOF delta) has become wider as well – an indication of increasing tradeoffs in DOF. Among the 81% of sub-cells with improved MEEF, 55% showed improved MEEF and improved DOF at the same time. Figure 9(c) indicates that increasing the weight of mask bias further from 0.5 to 0.7 does not produce a comparable amount of improvement in MEEF nor DOF as was seen when increasing the weight from

0.2 to 0.5. In fact, the percentage of sub-cells with improved MEEF and degraded DOF was increased by 3%, and the percentage of sub-cells with both improved MEEF and DOF was decreased by 1%. Based on the result in Figure 9, it can be concluded that: (i.) EDM-aware inversion can improve MEEF; (ii.) EDM-aware inversion has potential to improve both MEEF and DOF; and, (iii.) putting too much weight on mask bias during inversion optimization may adversely impact DOF. Therefore, when optimizing inversion variables to explore design rules, it is important to choose mask weighting carefully to balance MEEF and DOF.

2.4 Hotspot Check using ILT: Random Logic and Bitcell

Another way to quantify the benefit of adding mask bias to inversion optimization, i.e. EDM-aware inversion vs. ED-aware inversion, is to run a hotspot check on a real design layout. Figure 10 shows a real as-drawn design layout. We first ran the layout through two different inversion optimization loops, one with ED-aware inversion and the other with EDM-aware inversion, again using distributed computing. We then picked a MEEF hotspot from the ED-aware inversion result and displayed it in a pixel-based MEEF map. Next, we compared this MEEF map with the MEEF map generated from EDM-aware inversion. We did this comparison on two different hotspot locations in the design; one in a random logic area and the other in an SRAM bitcell.

Figure 11 shows a MEEF map of the random logic hotspot area. The result shows MEEF hotspots were eliminated when switching from ED-aware inversion to EDM-aware inversion. In the meantime, common DOF remained comparable, $0.135\mu\text{m}$ vs. $0.134\mu\text{m}$. The result supports the conclusion from Section 2.3 above, that mask-aware inversion can be used to reduce MEEF while maintaining DOF.

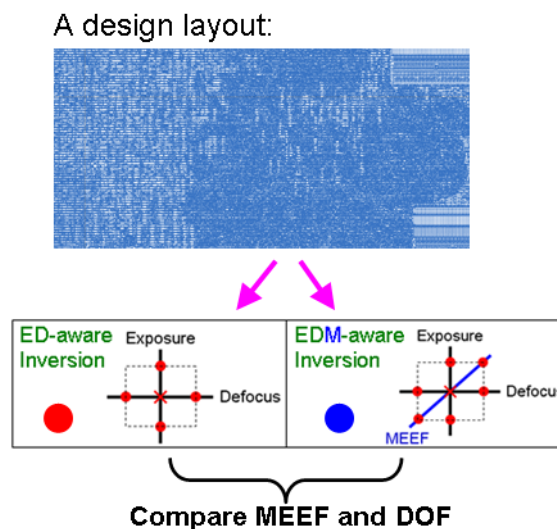


Figure 10. Hotspot check on a real design layout using ED-aware inversion and EDM-aware inversion.

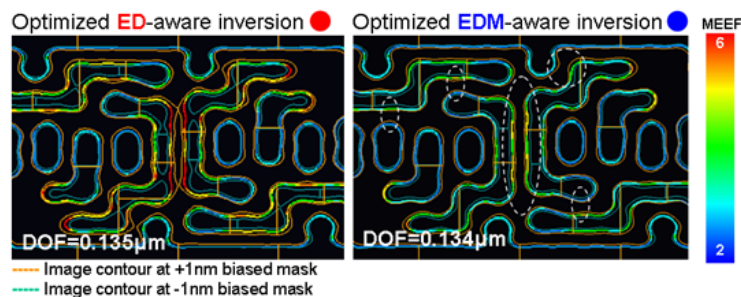


Figure 11. Hotspot check in a random logic using pixel-based MEEF maps (a) Hotspots were observed with ED-aware inversion (a) Hotspots were eliminated with EDM-aware inversion.

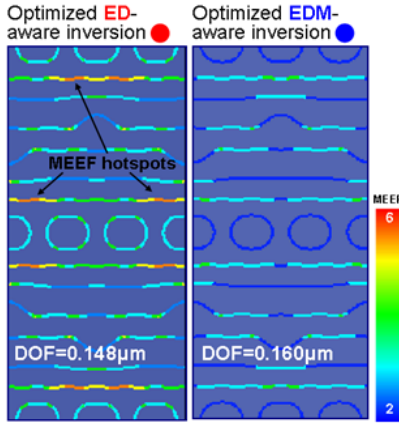


Figure 12. Hotspot check in a bitcell using pixel-based MEEF maps (a) Hotspots were observed with ED-aware inversion (b) Hotspots were eliminated with EDM-aware inversion.

Figure 12 shows MEEF maps of hotspots in a bitcell. The result shows MEEF hotspots were also eliminated when switching from ED-aware inversion to EDM-aware inversion. At the same time, common DOF was increased from $0.148\mu\text{m}$ to $0.160\mu\text{m}$. The result supports the observation in Section 2.3.

2.5 Design Rule (DR) Exploration using Real Design Layout

In the previous section, we demonstrated the utility of the ILT technique to quickly screen specific rule and process choices using large numbers of parameterized structures. There are several advantages to using parameterized structures to explore design rules. Parameterized structures are easier to create and can accommodate larger number of design variables. In addition, analysis of the result is more straightforward. However, there is a drawback about this approach - typical parameterized structures do not fully reflect patterning complexity of real design layouts, especially complex 2D metals. One way to narrow this gap is to perform design rule exploration directly on real design layouts and feed the result back to the initial design rules established from the parameterized approach. Figure 13 shows a typical parameterized metal line-end structure and, for comparison, a real design layout that tests the same rule.

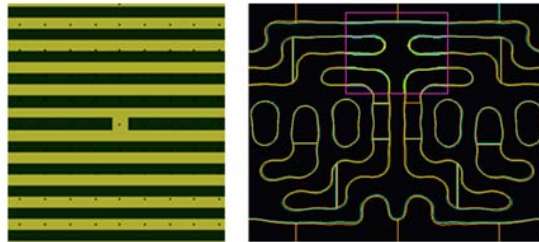
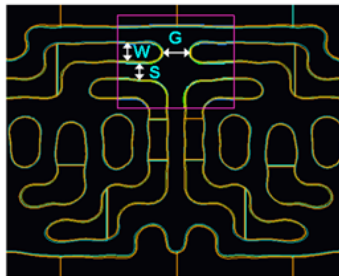


Figure 13. (a) A typical parameterized structure with metal line-end (b) A real design layout with metal line-end.



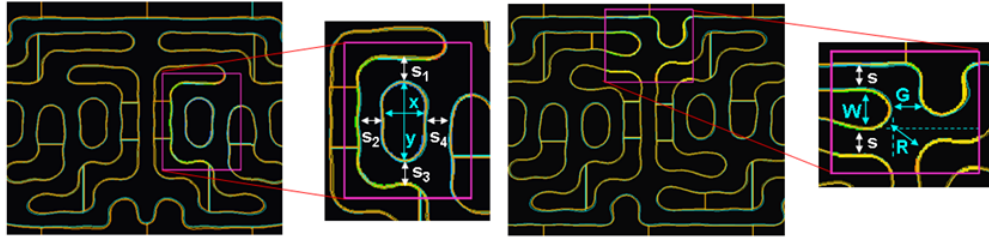


Figure 14. Applications of exploring design rules using real design layouts: (a) A layout with simple metal line-end. (b) A layout with metal landing pad. (c) A layout with complex metal line-end.

Figure 14 shows three test cases for exploring design rules using real design layouts. Figure 14(a) and Figure 14(c) both illustrate a layout with metal line-end. The application is to explore line-end conditions that allow densest possible interconnects. Figure 14(b) illustrates a layout with metal landing pad. The application is to explore conditions that enable the smallest possible metal landing pad. In this paper, only the simulation flow and simulation results from Figure 14(a) are presented.

Figure 15 shows the simulation flow for design rule exploration using a real design layout. The first step is to select an area of interest on a real design layout, a random logic in this case, to explore a particular set of design rules. Next, we define design variables and the allowed design space (range of variation) for each variable. We then populate topologies and run the layout through EDM-aware inversion using distributed computing as available in the simulation tool. We repeat the same analysis steps we presented earlier to extract an acceptable line-end space by comparing DOF and MEEF results to pre-defined criteria; $0.120\mu\text{m}$ DOF at 10% exposure latitude (EL) and 5.0 MEEF in this case. We then cross-check this line-end space number with the initial design rules to see if current design rules can support it. If the answer is “No,” the design rules are revised based on the requirements of the real design layout. Finally, we repeat this simulation flow with ED-aware inversion and compare its results with the results from EDM-aware inversion.

Figure 16 shows ED-aware and EDM-aware simulation results for line-end spaces. There are two key goals here. One is to quantify the improvement in lithographic performance when going from ED-aware inversion (red curve) to EDM-aware inversion (blue curve). The other is to find the minimum line-end space for which MEEF and DOF meet the pre-defined criteria. The result in Figure 16 shows clear improvement on MEEF and EL by going from ED-aware inversion to EDM-aware inversion. DOF is comparable between the two inversion approaches. The result also indicates that EDM-aware inversion can support a 56nm line-end space; whereas, ED-aware inversion cannot.

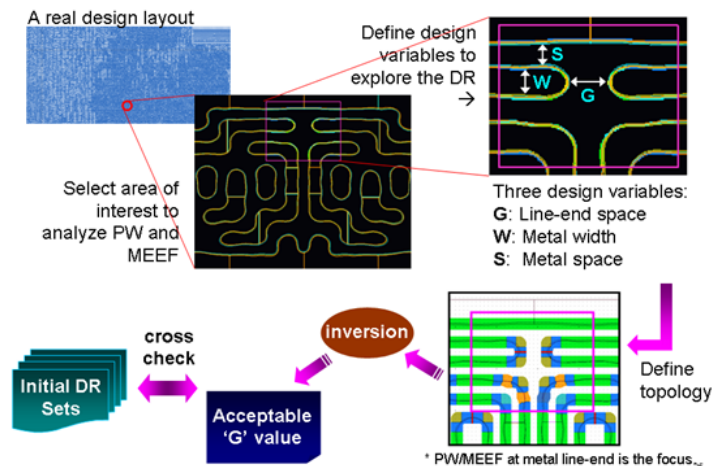


Figure 15. Simulation flow of design rule exploration using a read design layout.

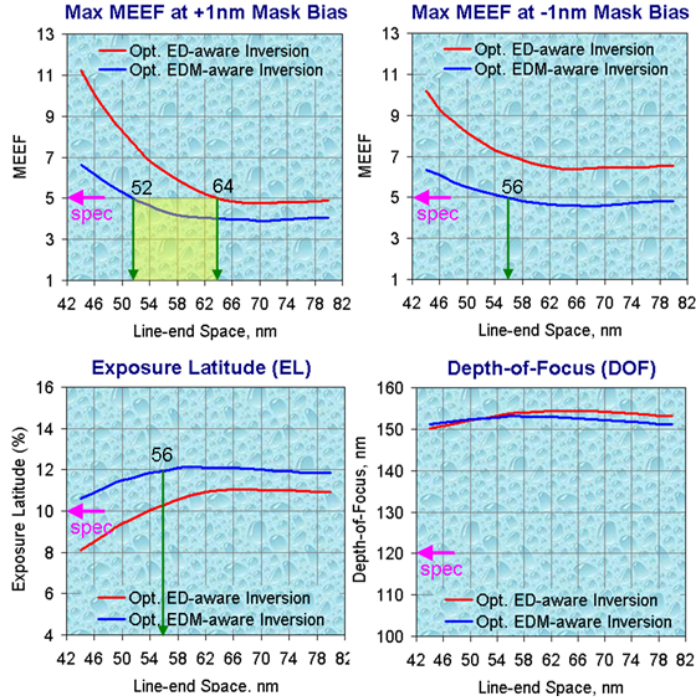


Figure 16. ED-aware vs. EDM-aware results vs. line-end spaces (a) Maximum MEEF at -1nm mask bias. (b) Maximum MEEF at +1nm mask bias. (c) Exposure latitude. (d) Depth-of-focus (DOF).

3. SUMMARY & CONCLUSIONS

A simulation tool utilizing inverse lithography techniques (ILT) has been employed to explore metal patterning options and their impact on 2D design rules (DR). In this paper, we showed the utility of ILT techniques to quickly screen metal line-end design rules and process choices – including illumination conditions and process bias – using large numbers of parameterized structures. The distributed computing capability in the simulation tool allowed experiments requiring large numbers of parameterized structures to be performed in reasonable time.

The same metal line-end parameterized structures were simulated to show MEEF and DOF variations when adding bias to mask optimization during the inversion (EDM-aware inversion). The study revealed that adding mask bias to the inversion optimization could improve both MEEF and DOF, with the amount of improvement depending on how highly mask bias was weighted during inversion optimization. The study shows putting too much weight on mask bias can produce adverse effects on DOF while only marginally improving MEEF. Therefore, for a given design rule, careful optimization of the inversion variables – exposure, defocus and mask bias – is important to find good balance between MEEF and DOF.

To further demonstrate the effectiveness of utilizing ILT techniques and EDM-aware inversion on metal patterning, a random logic layout and an SRAM bitcell were simulated again using distributed computation. Here, both MEEF and DOF were displayed in color bitmaps utilizing ILT’s pixel-based metrology. The study revealed that color bitmaps greatly facilitated detection and visualization of DOF and MEEF hotspots anywhere in the design. Color bitmaps also enabled effective comparisons of the results between different optimization runs. The study also confirmed that optimized EDM-aware inversion can improve MEEF with negligible trade-off in DOF at the same time.

Finally, a methodology was introduced to explore 2D metal design rules using real design layouts. Such methodology could help counter the fact that typical parameterized structures do not fully reflect patterning complexity seen in real design layouts. The simulation results from this methodology can be used to refine the initial design rules established from the parameterized approach, thereby improving the accuracy and quality of 2D rules while simultaneously accelerating learning cycles in the design phase.

4. REFERENCES

- [1] S. Abrams, et al., "Fast inverse lithography technology," Proc. of SPIE Vol. 6154 1J (2006).
- [2] L. Pang, et al., "Validation of inverse lithography technology (ILT) and its adaptive SRAF at advanced technology nodes." Proc. of SPIE Vol. 6924 0T (2008)
- [3] S. Prins, et al., "Inverse Lithography as a DFM Tool: Accelerating Design Rule Development with Model-Based Assist Feature Placement, Fast Optical Proximity Correction and Lithographic Hotspot Detection" Proc. of SPIE Vol. 6925 0E (2008).